WARSAW UNIVERSITY OF TECHNOLOGY

Ph.D. Thesis

Discipline of physical sciences
Field of natural sciences

Małgorzata Giza, M.Sc. Eng.

Interface engineering for scalable 2D material FETs: contact resistance, dielectric integration and large-area fabrication

Supervisor
Prof. **Mariusz Zdrojek**, PhD Eng.

Assistant supervisor
Michał Świniarski, PhD Eng.

Warsaw 2025

Funding

I would like to acknowledge support from the PRELUDIUM BIS 2 project (2020/39/O/ST5/00416) by the National Science Centre, Poland.

Acknowledgments

I would like to express my deepest gratitude to my supervisor, Prof. Mariusz Zdrojek, and to my co-supervisor, Dr. Michał Świniarski, for their constant guidance, valuable advice, and continuous encouragement throughout my doctoral studies. Their expertise, constructive feedback, and support at every stage of this work have been essential for the completion of this dissertation. I am especially grateful for teaching me how to work independently and critically, which has been an invaluable part of my scientific development.

I am also deeply thankful to Prof. Saptarshi Das for the opportunity to conduct research in his group and for giving me an alternative perspective on two-dimensional devices. His insights and mentorship have greatly enriched my scientific experience.

My heartfelt thanks go to my closest colleagues, who constantly reminded me to believe in myself. Especially I would like to thank: Krishnendu Mukhopadhyay, for the inspiring, often hours-long discussions, for encouraging me to continue my research and for his constant support; Arkadiusz Gertych for thought-provoking conversations, a deep and analytical perspective on problems, and for introducing me to the different types of exfoliation; and Karolina Czerniak-Łosiewicz for guiding me into the world of 2D materials and for sharing her knowledge and experience that helped me build a foundation in this field.

I would also like to thank all members of the NANOstructures Group at the Faculty of Physics, Warsaw University of Technology, for creating a supportive and stimulating atmosphere, which has made this journey both productive and enjoyable.

My sincere thanks also go to my colleagues from the Das Research Group at Penn State University, for continuous readiness to help, and for generously sharing their knowledge and expertise. It was a great experience to work and learn alongside you.

Finally, I wish to express my deepest gratitude to my family – especially my parents and siblings – as well as to my dear friends, for their unwavering support, patience, and for always listening to my stories about research. I could not have reached this point without your love and encouragement.

Streszczenie

Niniejsza rozprawa traktuje o roli interfejsów w rozwoju technologii urządzeń opartych na materiałach dwuwymiarowych. Skupia się na trzech głównych wyzwaniach współczesnej nanoelektroniki: pozyskiwaniu monowarstw o dużych powierzchniach, redukcji rezystancji kontaktów oraz integracji dielektryków o wysokiej stałej dielektrycznej.

W pierwszej części przedstawiono technikę eksfoliacji wspomaganej złotem, umożliwiającą otrzymywanie jednorodnych monowarstw MoS_2 i WSe_2 oraz budowę tranzystorów polowych i inwerterów w technologii CMOS. Następnie omówiono metodę transferu z użyciem złotej taśmy, prowadzącą do kontrolowanego formowania kontaktów $Au/MoS_2/WS_2$ i poprawy wstrzykiwania nośników ładunku. W ostatniej części zaprezentowano wykorzystanie samoutleniających się metalicznych warstw van der Waalsa jako matryc nukleacyjnych do depozycji cienkich dielektryków i wytwarzania tranzystorów z górną bramką.

Rozprawa podkreśla znaczenie projektowania interfejsów w kształtowaniu właściwości elektronicznych materiałów dwuwymiarowych i wskazuje kierunki dalszego rozwoju nanoelektroniki.

Słowa kluczowe: tranzystory polowe, materiały dwuwymiarowe, dichalkogenki metali przejściowych, rezystancja kontaktów, inżynieria interfejsu, dielektryki o wysokiej stałej dielektrycznej, matryce nukleacyjne, eksfoliacja asystowana złotem, wielkoformatowa integracja, nanoelektronika

Abstract

This dissertation addresses the role of interfaces in the development of device technologies based on two-dimensional materials. It focuses on three key challenges in modern nanoelectronics: obtaining large-area monolayers, reducing contact resistance, and integrating high-κ dielectrics.

The first part presents the gold-assisted exfoliation technique, which enables the preparation of uniform MoS_2 and WSe_2 monolayers and the fabrication of field-effect transistors and CMOS inverters. Next, a transfer method using gold tape is discussed, allowing for controlled formation of Au/MoS_2/WS_2 contacts and improved charge carrier injection. In the final part, the use of self-oxidizing van der Waals metal seed layers as nucleation templates for the deposition of thin dielectrics and the realization of top-gated transistors is demonstrated.

The dissertation highlights the importance of interface engineering in tailoring the electronic properties of two-dimensional materials and points to future directions for the advancement of nanoelectronics.

Keywords: field-effect transistors, two-dimensional materials, transition metal dichalcogenides, contact resistance, interface engineering, high-κ dielectrics, seed layers, gold-assisted exfoliation, large-area integration, nanoelectronics

Contribution of the author and collaborators to the conducted research

Gold-assisted exfoliation and transfer of 2D materials	**Małgorzata Giza**
PMMA-assisted transfer of 2D materials	Ziheng Chen **Małgorzata Giza**
Electrical characterization	**Małgorzata Giza** (results in Chapter 4, 5 and 6) Krishnendu Mukhopadhyay (results in Chapter 4, 6)
Electron beam lithography	**Małgorzata Giza** (results in Chapter 4, 5 and 6) Ziheng Chen (results in Chapter 6)
Photolithography	Pranavram Venkatram **Małgorzata Giza**
Metal deposition	**Małgorzata Giza**
Atomic layer deposition	Ziheng Chen **Małgorzata Giza**
Raman spectroscopy and PL	**Małgorzata Giza**
AFM	**Małgorzata Giza** Krishnendu Mukhopadhyay
XPS	Bob Hengstebeck
TEM and EDX	Ding Lei
SEM	**Małgorzata Giza**
MOCVD	Rohini Sanikop Chen Chen Joan M Redwing
TMDs bulk crystal growth	Iva Plutnarová Jan Luxa Zdenek Sofer

Table of contents

Chapter 1. Introduction

1.1. Overview of 2D materials for nanoelectronics

Two-dimensional (2D) semiconductors, especially transition-metal dichalcogenides, TMDs, such as MoS_2 and WSe_2, have emerged as promising channel materials for future electronics. Their atomically thin layers (e.g. monolayer MoS_2 is only 6.15 Å thick[1]) can offer ultimate electrostatic control of the channel. Thinning silicon below ~10 nm severely degrades carrier mobility due to surface scattering[2], whereas 2D layers inherently avoid this issue: they maintain relatively high mobility even at monolayer thickness[3–5]. The extent to which field-effect transistors (FETs) can be scaled down is limited by short-channel effects that originate from the fundamental properties of the semiconductor materials. Monolayer thickness enables ultimate vertical scaling and mitigates short-channel effects when properly gated[6,7]. Advanced simulations predict that MoS_2 transistors could exhibit much lower OFF-state leakage and less mobility degradation than silicon when scaled to sub-5 nm gate lengths[8].

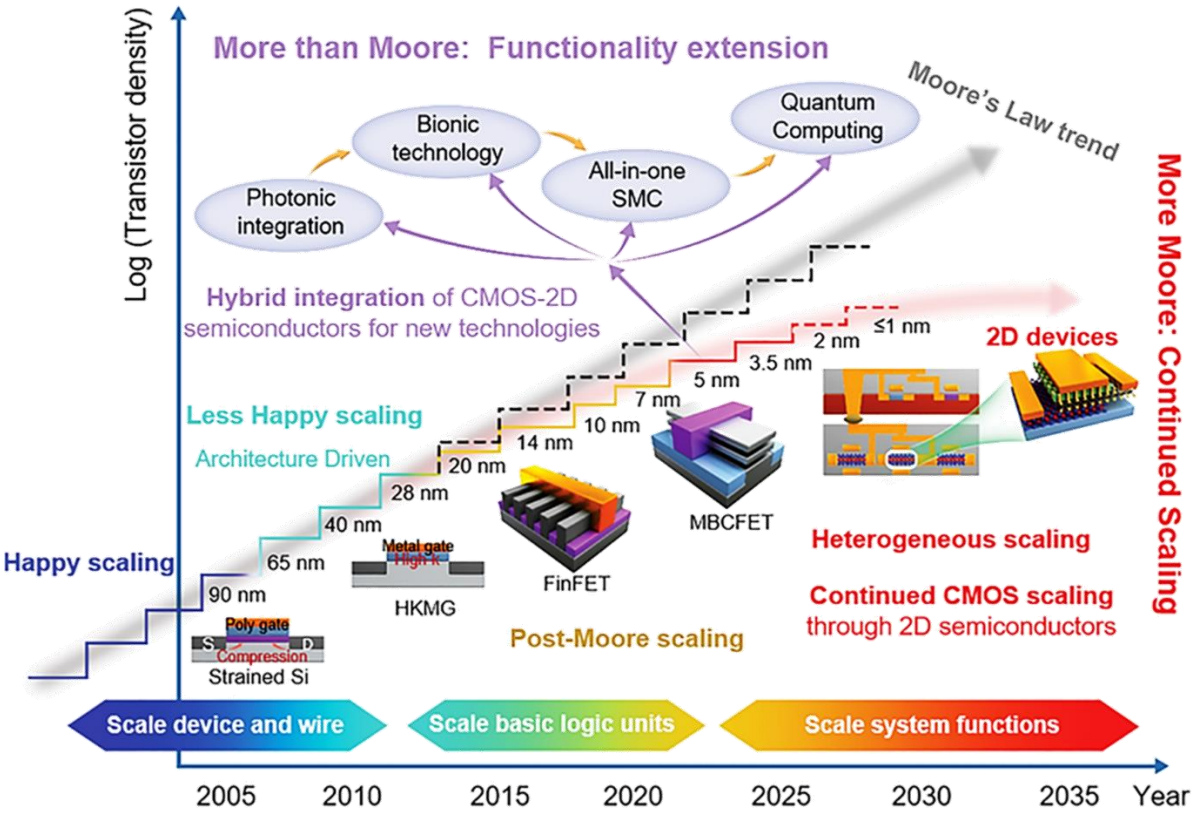

Figure 1 *Conceptual diagram highlighting the potential contributions of 2D materials to next-generation semiconductor technologies. In addition to supporting continued scaling of devices consistent with Moore's Law ("More Moore"), 2D materials provide new avenues for heterogeneous integration and unconventional device architectures that merge digital and analog functionalities ("More than Moore")[9].*

In addition, TMDs have clean, dangling-bond-free surfaces, which enable sharp and defect-minimized interfaces. These properties together imply that 2D TMD channels could sustain very short gate and channel lengths with robust ON/OFF current ratios and steep subthreshold slopes, potentially extending "More Moore" scaling beyond the limits of bulk semiconductors (**Figure 1**)[10].

Key advantages of TMDs compared with bulk silicon include not only ultra-thin channels and high intrinsic mobility, but also direct bandgaps and compatibility with van der Waals heterostructure integration. Many semiconducting TMD monolayers exhibit direct bandgaps of 1.1–2.1 eV[11], enabling efficient gate modulation and creating opportunities for optoelectronic integration, in contrast to the indirect bandgap of bulk silicon. Furthermore, the layered structure and absence of dangling bonds make it possible to stack 2D layers without lattice matching constraints, which opens the way to novel device architectures such as vertical or heterojunction devices not easily attainable with 3D materials. Additionally, the monolithic 3D integration of 2D materials allows for wafer-scale stacking of functional layers, facilitating the development of multifunctional devices with reduced interconnect delays and enhanced performance, in line with the "More than Moore" approach (**Figure 1**)[12].

1.2. Motivation and challenges in device fabrication

Although 2D FETs hold great promise, realizing their performance in practice faces several challenges, including high contact resistance, non-ideal gate-dielectric interfaces, and issues with scalability and reproducibility when targeting wafer-scale device fabrication. For instance, at a metal–2D interface the formation of a Schottky barrier is commonly observed, resulting from Fermi-level pinning near the TMD's band edges. This barrier can significantly impede carrier injection, raising the contact resistance and power loss[11,13]. Without perfect junctions, a large fraction of the applied bias drops at the contacts, reducing the ON-current and effective mobility. Surface states or defects at the contact interface can further pin the Fermi level, making it difficult to choose a metal that yields low resistance[14]. In bulk silicon, such problems were solved by heavy doping at the contacts; this is not easily done in atomically thin 2D channels. Conventional ion-implantation and diffusion doping techniques are incompatible with monolayer semiconductors, making it difficult to not only dope contact regions but also to achieve stable p-type conduction or complementary (CMOS) operation in materials like MoS_2 or WSe_2[15]. Experimental workarounds such as molecular charge-transfer doping or electrostatic gating can temporarily tune carrier type, but a robust and permanent solution for doping control in 2D channels remains elusive. In addition to these interfacial and doping issues, further

complications such as environmental stability, short-channel effects, and limited thermal management capacity continue to hinder the practical deployment of 2D FETs. Similarly, integrating high-quality gate dielectrics with 2D channels is difficult. A pristine TMD surface has no dangling bonds, so conventional atomic layer deposition (ALD) precursors do not adsorb uniformly. Early ALD on unmodified MoS2 often produces island-like, oxides with high leakage current[16]. This results in interfaces with high trap density, gate leakage, and hysteresis, undermining device performance. Metal seed layers (e.g. evaporated Ta, Al) can promote ALD nucleation, but these often introduce their own problems (interfacial roughness, unintentional doping or charge traps)[17]. This poor interface leads to reduced gate capacitance, threshold shifts, and larger subthreshold swing. Achieving an ultra-thin, uniform high-κ dielectric on 2D channels - while preserving interface cleanliness - is thus a major integration bottleneck. Inadequate gate-insulator integration not only increases interface traps (leading to hysteresis), but also hinders aggressive scaling of 2D FETs due to device variability[18].

Another critical bottleneck is the reproducible fabrication of devices on large areas. While the highest-performing 2D FETs are still obtained from exfoliated flakes or small-area CVD films, these approaches lack scalability. Transitioning to wafer-scale growth and processing inevitably introduces structural non-uniformities such as grain boundaries, wrinkles, and thickness variations, all of which degrade device yield and performance consistency. For example, grain boundaries in CVD-grown monolayer MoS_2 act as scattering sites that reduce carrier mobility and contribute to device-to-device performance variability[19,20]. Ensuring uniform, crack-free monolayer coverage over an entire wafer is extremely difficult; even microscopic wrinkles or thickness patches can significantly alter a transistor's threshold voltage or ON-current. These non-idealities ultimately limit manufacturing yield and consistency of 2D devices. Current integration strategies are therefore not yet compatible with established high-volume semiconductor manufacturing, limiting the path from laboratory prototypes to practical technologies.

Beyond material interfaces and uniformity, 2D devices also face reliability and process-integration challenges. Many 2D semiconductors are highly sensitive to their environment: exposure to oxygen, moisture, or other ambient species can induce oxidation and charge trapping, leading to performance degradation over time[21]. For instance, unpassivated MoS_2 films have been shown to oxidize and increase in resistance by several-fold within months of air exposure. Encapsulating the 2D channel with an inert overlayer (such as hBN – hexagonal boron nitride) is therefore often required to preserve long-term stability. Furthermore,

integrating 2D FETs into conventional CMOS process flows presents its own difficulties. High-quality 2D material synthesis typically requires excessively high temperatures (often >700 °C) that exceed the thermal budget of semiconductor back-end-of-line processing (~450 °C)[22]. Thus, many device fabrication steps must be performed at reduced temperatures to avoid damaging the atomically-thin layers. Chemical compatibility is another concern, as standard etchants or cleaning agents can inadvertently remove or degrade 2D films. Developing low-temperature, 2D-friendly fabrication techniques is essential for monolithic integration of 2D FETs with silicon electronics.

At the device architecture level, scaling down the channel length in 2D FETs can lead to short-channel effects similar to those in bulk CMOS transistors. The ultra-thin body of a 2D transistor does improve electrostatic gate control, enabling channel lengths on the order of only a few nanometers. However, at such scaled dimensions, phenomena like drain-induced barrier lowering (DIBL), threshold voltage roll-off, and increased OFF-state leakage are still observed. Mitigating these effects likely requires design innovations such as multi-gate or junction-free device architectures, since creating abrupt source/drain doping profiles is not feasible in 2D materials. In addition, thermal management is inherently more challenging in nanodevices with 2D channels. The minimal thickness of the active layer means heat cannot spread vertically, and the thermal boundary resistance at the 2D/substrate interface is high. As a result, self-heating and hot spots may occur even at moderate power densities, potentially accelerating device failure. Efficient heat dissipation - through improved interfaces or better thermally conductive substrates - will be crucial for reliable high-power operation of 2D electronics.

These challenges highlight the need for systematic approaches that can both mitigate current device limitations and clarify the physical origins of those limitations. High contact resistance constrains current drive, imperfect dielectric integration undermines gate control, and limited scalability hampers any realistic transition from laboratory demonstrations to manufacturable technologies. Addressing these issues is therefore essential not only for pushing the performance of individual 2D FETs but also for determining whether 2D semiconductors can truly serve as a platform for next-generation electronics. The present dissertation is driven by this dual motivation: to uncover practical bottlenecks in device performance and fabrication while simultaneously exploring the fundamental mechanisms that give rise to them.

1.3. Scope and objectives of the dissertation

The central objective of this dissertation is to investigate fundamental challenges associated with the integration of two-dimensional materials into electronic devices. Rather than focusing solely on improving transistor performance, the work explores key issues that determine how 2D systems operate, including charge injection at metal/semiconductor interfaces, the nucleation and growth of high-quality dielectric layers on inert 2D surfaces, and the scalable preparation of monolayers with controlled geometry. Particular emphasis is placed on understanding the underlying physical mechanisms that govern these processes, as this knowledge is essential for predicting device behavior and explaining the physical origins of performance limitations. These aspects are not only critical for field-effect transistors but also broadly relevant to a range of other 2D-based device concepts. The thesis is organized around three complementary studies, each designed to provide deeper insight into the mechanisms that limit device functionality and to outline possible strategies for overcoming them.

Study 1: Large-area gold-assisted exfoliation of TMDs monolayers for complementary 2D FETs

In the first study, gold-assisted mechanical exfoliation is used to obtain large-area monolayer flakes of MoS_2 and WSe_2 directly from bulk crystals. Using these materials, 120 n-channel (MoS_2) and 120 p-channel (WSe_2) transistors are fabricated, yielding a broad statistical dataset that enables a comprehensive analysis of device performance, including, for the first time, the characteristics of p-type FETs produced by this method. These monolayer FETs are further integrated to construct and evaluate complementary metal-oxide-semiconductor (CMOS) inverters, demonstrating the viability of this approach for functional circuits. This study establishes gold-assisted exfoliation as an effective technique for isolating monolayers in large areas while maintaining good device performance, highlighting its potential for scalable fabrication of 2D devices, while also revealing limitations that may hinder its straightforward adoption in truly large-scale manufacturing.

Study 2: Contact resistance engineering in TMD-based FETs using vdW interlayer

The second study introduces a thin monolayer interlayer at the metal/semiconductor interface to reduce contact resistance in WS_2 transistors. Specifically, a MoS_2 monolayer is placed under the source/drain contacts of a WS_2 channel, forming an Au/MoS_2/WS_2 junction. This 2D–2D junction exploits Fermi-level pinning (FLP) to lower the Schottky barrier at the contacts, thereby reducing contact resistance and enhancing overall FET performance. Using a gold-

assisted transfer technique, method specifically developed for this study, such monolayer heterostructures are fabricated with prepatterned geometries to ensure precise placement of the interlayer. A statistical study of 160 FET devices - with and without the under-contact interlayer - consistently shows that devices with the interlayer have improved performance and underscores the critical influence of contact resistance on key FETs metrics. Collectively, this work demonstrates that engineering a 2D–2D interface (rather than relying solely on a conventional metal–semiconductor contact) is a viable and scalable strategy for improving contact performance in 2D devices.

Study 3: Gate dielectric integration enabled by vdW metal seed layers in 2D FETs

The third study addresses the challenge of integrating high-κ gate dielectrics on 2D semiconductors by using monolayer van der Waals (vdW) metals as ultrathin seed layers for ALD. Monolayers of vdW metals such as $TaSe_2$, $TaTe_2$, $NbSe_2$, $NbTe_2$, $PdSe_2$, and $PtSe_2$ spontaneously oxidize in air to form uniform oxides films ideally suited for initiating ALD of high-κ dielectrics on 2D materials. When employed as interfacial layers on monolayer MoS_2 and WSe_2, these oxidized vdW metal layers enable conformal deposition of high-κ dielectrics (HfO_2, ZrO_2, Al_2O_3) with high breakdown fields and low leakage currents. Notably, the oxidized vdW monolayer itself exhibits a high dielectric constant, yielding gate stacks with excellent electrostatic control and negligible gate leakage. Because many vdW metals can be synthesized via scalable methods (such as chemical vapor deposition), even on other 2D materials like MoS_2 or WSe_2, this approach is promising for wafer-scale integration of top-gated 2D transistors with reliable gate dielectrics.

Together, these three studies provide complementary strategies for overcoming critical challenges in 2D electronics. By integrating contact engineering, large-area material preparation (via gold-assisted exfoliation), and controlled dielectric deposition (using ALD facilitated by vdW seed layers), this dissertation outlines a framework for scalable fabrication of high-performance 2D devices. The findings not only advance the understanding of how contacts and interfaces affect 2D FETs behavior, but also point to practical routes for realizing high-performance, complementary (n- and p-type) 2D devices within existing semiconductor manufacturing processes. This work highlights how carefully engineered 2D material heterostructures can bridge the gap between fundamental materials research and real-world applications in future nanoelectronics.

Chapter 2. Fundamentals of 2D materials and device physics

2.1. Electronic and structural properties of monolayer semiconducting TMDs

Semiconducting TMDs (MX_2, M – transition metal, X - chalcogen) like MoS_2, WS_2, and WSe_2 crystallize in layered structures where each monolayer consists of a plane of metal atoms between two planes of chalcogen atoms. In the common 2H phase, the metal atoms occupy trigonal prismatic sites coordinated by six surrounding chalcogen atoms (**Figure 2**), and this coordination imparts the semiconducting 2H phase with structural stability. Adjacent TMD layers are held together by weak van der Waals forces without any covalent bonding or surface dangling bonds. As a result, TMD monolayers can be mechanically exfoliated from bulk crystals and restacked arbitrarily, and their pristine surfaces remain chemically inert due to the absence of dangling bonds. These structural characteristics yield an atomically flat semiconductor sheet, which is highly advantageous for both fundamental studies and device integration.

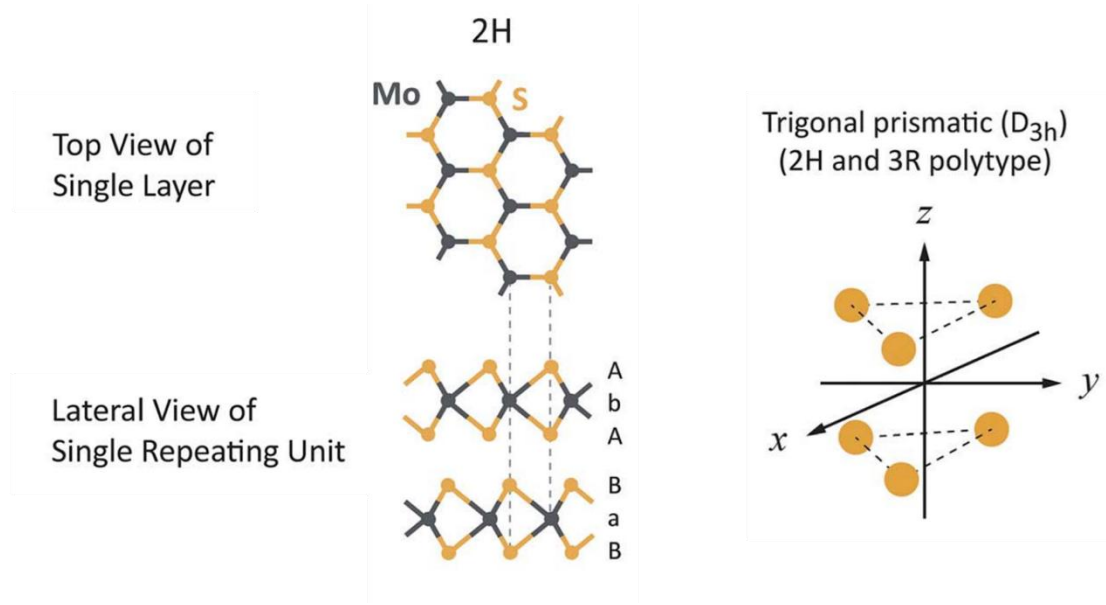

Figure 2 *Schematic crystal structure of 2H MoS_2 polytype with trigonal prismatic coordination*[23].

Monolayer TMDs exhibit electronic properties distinct from their bulk counterparts due to quantum confinement and symmetry changes. Notably, most of the group-VI TMD monolayers (MoS_2, WS_2, $MoSe_2$, WSe_2, etc.) possess a direct band gap in the range of ~1.6–2 eV, which corresponds to optical transitions within the visible spectrum, whereas their bulk or few-layer forms have indirect band gaps[24]. For example, bulk 2H–MoS_2 is an indirect-gap semiconductor

(~1.2 eV gap) with its valence band maximum at the Γ-point and conduction minimum at an off-center point, but a single MoS_2 layer has a direct gap of ≈1.9 eV with both band extrema at the K-points of the Brillouin zone (**Figure 3**). Similarly, monolayer WS_2 and WSe_2 have direct gaps of roughly 2.0 eV and 1.6–1.7 eV, respectively, compared to much smaller indirect gaps (~1.3 eV for WS_2, ~1.2 eV for WSe_2) in the bulk phase[25].

Density functional studies reveal that the electronic states at the band edges in those materials are derived primarily from the metal d-orbitals. In particular, the lowest conduction band is dominated by the metal out-of-plane d_{z^2} orbital, while the top of the valence band arises largely from in-plane $d_{x^2-y^2}$ and d_{xy} orbitals of the metal[26]. This orbital composition and the reduced dimensionality give rise to effective masses that are larger than in graphene or III–V semiconductors, reflecting flatter band dispersions and reduced carrier velocities[27]. At the same time, the masses are not excessively heavy, which means charge carriers can still move efficiently within the 2D plane. Calculations and measurements find electron effective masses on the order of $m \sim 0.55\ m_0$ (in units of the free electron mass) in monolayer MoS_2. WS_2 has even lower (~0.46 m_0) effective electron mass due to the broader bands. In contrast, WSe_2 tends to have lighter holes (≈0.44 m_0)[28]. These distinctions translate into different device polarities: MoS_2 is typically employed as an n-type semiconductor due to its relatively light electron band, WSe_2 is better suited for p-type conduction owing to its more favorable valence band, while WS_2, with its lighter electron effective mass and wide bandgap, is predominantly n-type but can also exhibit ambipolar behavior under suitable electrostatic gating or contact engineering. The relatively larger effective masses imply stronger carrier localization in momentum space compared to light-mass semiconductors (e. g. GaAs, InAs[29]), which leads to reduced mobility but also a higher density of states near the band edges. This balance is crucial for transistor operation, as it ensures sufficient current drive while also enhancing electrostatic control and suppressing short-channel effects in ultra-thin devices.

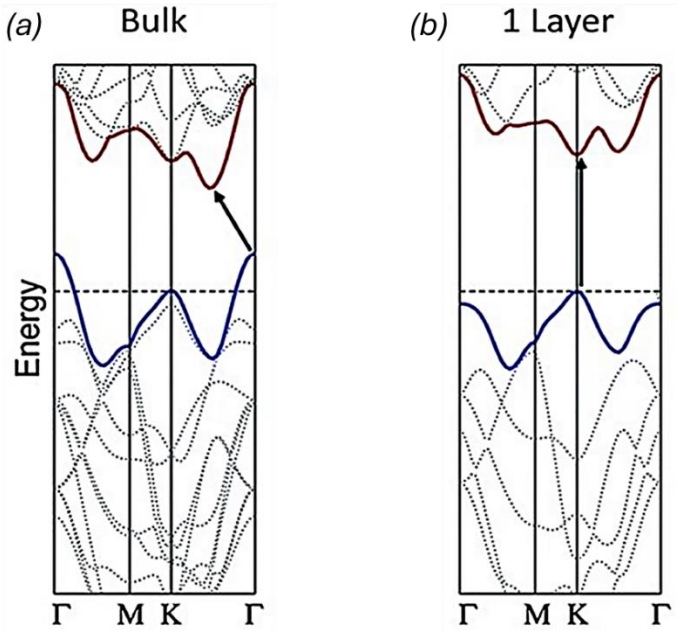

Figure 3 *Band structure of (a) bulk with marked indirect bandgap and (b) monolayer MoS_2 with marked direct bandgap*[30] .

Monolayer TMDs demonstrate remarkable optical properties stemming from their direct band gaps and strongly bound excitons. As direct-gap semiconductors, single layers of MoS_2, WS_2, WSe_2, etc., absorb and emit light efficiently in the visible spectral range. The optical absorption in a monolayer is unusually strong - a single pass can absorb up to ~20% of incident light at resonance - owing to the high oscillator strength of the band-edge transitions[31]. Conversely, in multi-layer or bulk TMDs the photoluminescence (PL) is extremely weak because the band gap becomes indirect, requiring phonon-assisted recombination. When thinned to one layer, the PL intensity of these TMDs increases by three to four orders of magnitude[32], reflecting the emergence of a direct radiative recombination pathway. Another signature of the 2D form is the prominence of excitonic effects. The Coulomb interaction is only weakly screened in a monolayer, yielding tightly bound excitons with large binding energies. As a result, the optical spectra are dominated by exciton resonances even at room temperature. In monolayer MoS_2 (and its congeners), the lowest energy optical transition is denoted the A exciton, which involves the upper valence band and conduction band at K. The B exciton, at a slightly higher energy, originates from transitions from the split-off lower valence sub-band to the same conduction band. The energy separation between the A and B exciton peaks directly reflects the valence band spin–orbit splitting. These pronounced A and B exciton features have been observed in absorption and photoluminescence spectra. Taken together, the direct-gap nature

and strong luminescence of monolayer TMDs highlight their potential not only for electronic devices but also for optoelectronic applications such as photodetectors and LEDs.

2.2. Field-effect transistors (FETs) principles

The operation of FETs relies on electrostatic control of charge carriers in a semiconducting channel through a gate electrode. When implemented with 2D materials, these devices follow the same general principles as bulk FETs, while their ultrathin geometry introduces distinct electrostatic and contact phenomena. **Figure 4a** presents a schematic of a back-gated 2D FET (using monolayer TMDs as the channel). The ultrathin channel sits on a dielectric atop a conductive substrate (back-gate), with metal source (S) and drain (D) contacts. The channel length L (distance between source and drain) and width W set the current-carrying capacity. The gate electrode is separated from the channel by a dielectric layer (usually SiO_2, HfO_2, Al_2O_3), which defines the gate capacitance. In operation, the gate electrode modulates charge in the channel, while source and drain electrodes inject and collect carriers. Because 2D channels are atomically thin (often <1 nm), they are usually fully depleted by gate fields, and the Debye length (screening distance in the semiconductor) often exceeds the channel thickness. In practice, the S/D regions in 2D FETs cannot be heavily doped as in bulk semiconductors. Instead, nearly ohmic behavior is achieved by using metallic 2D materials, locally induced metallic phases, or carefully selected contact metals, while the channel remains intrinsic or lightly doped to minimize scattering.

Figure 4b-d illustrate the fundamental electrostatic and transport behavior of an ideal 2D-FET. **Figure 4b** shows the transfer characteristics source-drain current I_{DS} versus gate voltage V_{GS} together with the schematic representation of the conduction band (CB) and valence band (VB) modulation induced by the applied gate voltage for n-type and p-type devices. The applied V_{GS} shifts the band edges: in the OFF state, the large barrier suppresses thermal carrier injection into the channel, whereas in the ON state, the barrier is lowered, enabling carrier transport from source to drain and leading to a sharp increase in I_{DS}. **Figure 4c,d** present the ideal output characteristics I_{DS} versus V_{DS} for p-type and n-type operation at different V_{GS} values. The output curves exhibit distinct linear and saturation regimes, which are characteristic features of

field-effect transistor operation. The linear regime appears only when the source–drain contact is ohmic, ensuring efficient carrier injection.

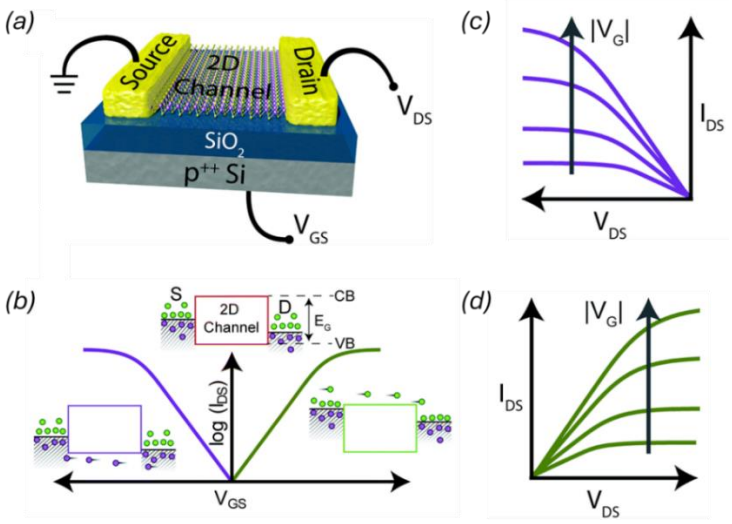

Figure 4 (a) *Schematic of the monolayer MoS_2 back-gated FET.* ***(b)*** *Transfer curve of a p-type and n-type 2D-FET, with the inset illustrating how the applied gate voltage shifts the conduction band and valence band. Output characteristics of* ***(c)*** *p-type FET and* ***(d)*** *n-type FET for different gate voltages*[24].

As it was mentioned before, applying a gate voltage V_{GS} modulates the carrier density in the atomically thin semiconducting channel. Because the entire channel thickness is comparable to or smaller than the Debye length, the gate field penetrates through the whole layer. In monolayer FETs, the electrostatic action of the gate directly changes the two-dimensional sheet carrier density n_{2D} across the entire atomic thickness of the channel. For an ideal capacitor model the induced sheet density is proportional to the effective gate capacitance C_g and the gate overdrive voltage ($V_{GS}-V_{TH}$) as stated in **Equation 1**:

$$n_{2D} = \frac{C_g}{q}(V_{GS} - V_{TH}) \qquad \textbf{Equation 1}$$

here, q is the elementary charge and V_{TH} is the threshold voltage. V_{TH} is the gate potential at which the channel becomes sufficiently populated with electrons to produce a measurable drain current.

Accumulation in an n-type monolayer MoS_2 channel refers to the gate-induced increase of electron density (**Figure 5a**), which leads to a rise of the Fermi level in the channel. When V_{GS} exceeds V_{TH} the channel enters the accumulation regime and the device conducts: the channel resistance decreases, the drain current I_{DS} rises, and carrier transport is limited by mobility and contact resistances. Depletion corresponds to the reduction of electron density when V_{GS}

approaches or falls below V_{TH}, leading to a lowering of the Fermi level in the channel (**Figure 5b**). In a monolayer, the depletion does not form a volumetric space-charge region as in bulk devices; instead, the entire 2D layer is depleted of carriers uniformly. Practical device behavior is further shaped by contacts and electrostatic environment. Large Schottky barriers or poor charge injection at the source/drain can mask the intrinsic accumulation/depletion response of the channel: measured I_{DS} may be contact-limited rather than channel-limited.

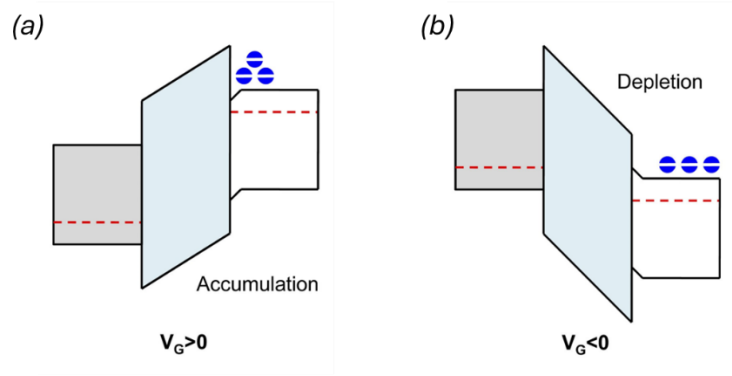

Figure 5 *Energy band diagrams of MoS_2 n-type FET illustrate the electrical gating effect for* ***(a)*** *the ON state and* ***(b)*** *the OFF state*[33].

The source–channel and drain–channel interfaces act as metal–semiconductor junctions. Ohmic contacts are designed so that the barrier to carrier injection is negligible, yielding a linear I_{DS}–V_{DS} relationship. Achieving ohmic behavior in 2D FETs does not rely on heavy doping, but instead on selecting contact materials or engineering 2D–2D interfaces that minimize the Schottky barrier and reduce Fermi-level pinning. Approaches include choosing metals with appropriate work functions, using metallic 2D phases or van der Waals contacts, and locally inducing high carrier densities near the contact regions. By contrast, a Schottky contact has a significant barrier height (Φ_B) and shows rectifying behavior. The ideal case, where Fermi level pinning effect is neglectable, electron (Φ_{Bn}) and hole (Φ_{Bp}) Schottky barrier is represented by Schottky-Mott **Equation 2** and **Equation 3**:

$$\Phi_{Bn} = \Phi_M - \chi \qquad \textbf{Equation 2}$$

$$\Phi_{Bh} = E_g - \Phi_{Bn} \qquad \textbf{Equation 3}$$

Where Φ_M - metal work function, χ - semiconductor electron affinity and E_g – bandgap energy.

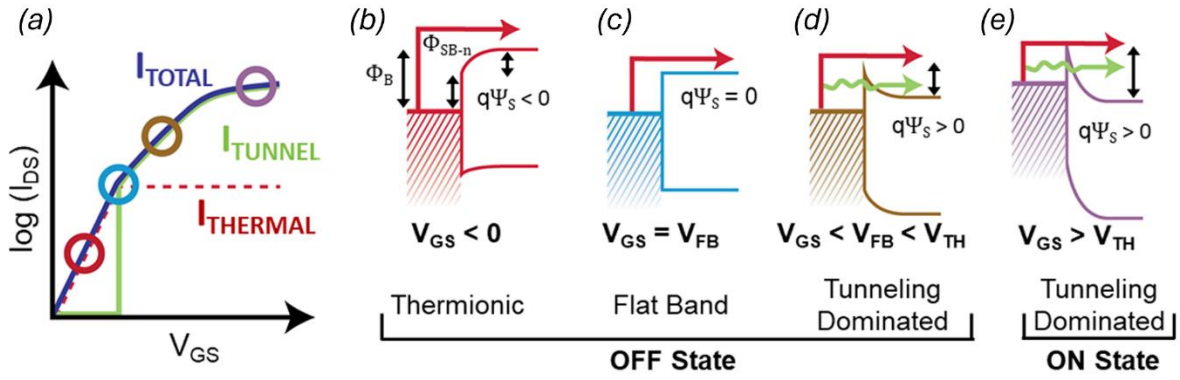

Figure 6 (a) *Representative transfer curve of an n-type 2D FET. The highlighted points mark different transport regimes: thermionic emission (red), flat-band alignment (blue), tunneling-dominated OFF state (brown), and tunneling-dominated ON state (purple). The corresponding band diagrams are illustrated in* ***(b)–(e)***[24].

Figure 6a shows transfer characteristic of n-type FET, which, as it was mentioned before, represents the dependence of I_{DS} on applied V_{GS}. I_{DS} arises from two distinct mechanisms: thermionic emission ($I_{THERMAL}$) of carriers surmounting the Schottky barrier, and thermally assisted tunneling (I_{TUNNEL}) of carriers going through the barrier. Both current components are strongly influenced by the gate voltage, which governs the electrostatic potential in the semiconductor channel via the surface potential ($q\Psi_S$). The thermionic current, $I_{THERMAL}$, is described by **Equation 4**:

$$I_{THERMAL} = AT^2 \exp\left(\frac{q\Phi_B}{k_B T}\right) \qquad \textbf{Equation 4}$$

where A denotes the Richardson constant, T is the temperature, k_B the Boltzmann constant, and Φ_B the effective injection barrier. This effective barrier is given as the sum of the intrinsic Schottky barrier height ($\Phi_{SB\text{-}n}$) and the surface potential. Surface potential is describe with **Equation 5**:

$$q\Psi_S = \left|\frac{V_{GS} - V_{FB}}{\gamma}\right| \qquad \textbf{Equation 5}$$

$$\gamma = 1 + \frac{C_s + C_{IT}}{C_{OX}} \qquad \textbf{Equation 6}$$

where V_{FB} representing the flat-band voltage, γ the inverse band-bending factor, and C_S, C_{IT}, and C_{OX} the semiconductor, interface-trap, and oxide capacitances, respectively. In the case of a fully depleted ultra-thin channel, it is reasonable to approximate $C_S \approx 0$ when the device operates in the OFF state. Within the thermionic regime (**Figure 6b**), $I_{DS} \approx I_{THERMAL}$, leading to an exponential dependence of current on gate bias. The exponential rise in I_{DS} continues until the flat-band voltage is reached, beyond which the thermionic component saturates and

becomes nearly independent of V_{GS} (**Figure 6c**). For gate voltages exceeding V_{FB}, the channel energy profile evolves (**Figure 6d–e**), allowing for thermally activated tunneling through the barrier. The tunneling contribution, I_{TUNNEL}, is quantified in **Equation 7**:

$$I_{TUNNEL} = \frac{2q}{h}\int_{q\Psi_S}^{\Phi_{SBn}} f(E)M_{2D}(E)T_{WKB}(E)dE \qquad \textbf{Equation 7}$$

where h denotes Planck's constant, f(E) the Fermi–Dirac distribution in the contact metal, $M_{2D(E)}$ the density of 2D transport modes in the channel, and $T_{WKB(E)}$ the barrier transmission probability evaluated under a triangular potential using the Wentzel–Kramers–Brillouin approximation and described in **Equation 8** and **Equation 9**:

$$M_{2D}(E) = \frac{2\sqrt{2m^*(E - q\Psi_s)}}{h} \qquad \textbf{Equation 8}$$

$$T_{WKB}(E) = exp\left(-\frac{8\pi}{3h}\sqrt{2m^*(\Phi_{SBn} - E)}\frac{\lambda_{SB}}{q\Psi_S}\right) \qquad \textbf{Equation 9}$$

\Where m* - the carrier effective tunneling mass and λ_{SB} - width of Schottky barrier.

In this transport regime (**Figure 6d**), the total current is the sum of the saturated thermionic component and the tunneling component, i.e. $I_{DS} = I_{THERMAL} + I_{TUNNEL}$. When the gate voltage is sufficiently large (ON-state operation), carrier transport is governed almost entirely by the tunneling component (**Figure 6e**). V_{TH} is therefore identified as the gate bias beyond which additional band bending no longer occurs, such that the surface potential effectively saturates.

The performance of 2D FETs is commonly assessed through a set of transport metrics that reflect both intrinsic channel properties and extrinsic interface effects. A first indication of switching capability is given by the ON-current (I_{ON}) and OFF-current (I_{OFF}). The ON-state current, measured at high gate bias, reflects the efficiency of carrier injection and transport in the channel, while the OFF-state current indicates the degree of leakage suppression when the device is nominally turned off. Their ratio I_{ON}/I_{OFF} is often emphasized as a compact measure of switching quality, demonstrating the ability of atomically thin channels to combine strong gate control with low standby power consumption.

The sharpness of the transition between these two states is captured by the subthreshold swing (SS), defined as the required gate voltage change to increase the drain current by one decade and can be describe by equations **Equation 10**, **Equation 11** and **Equation 12**:

$$SS = \frac{mk_BT}{q}\ln(10) \quad \textbf{Equation 10}$$

$$m = \left(1 + \frac{C_S}{C_{OX}} + \frac{C_{IT}}{C_{OX}}\right) \quad \textbf{Equation 11}$$

$$C_{IT} = qD_{IT} \quad \textbf{Equation 12}$$

where D_{IT} is the interface trap density.

In ideal conditions, this slope approaches the thermal limit of 60 mV/dec at room temperature, but in real 2D FETs it is typically larger due to the presence of interface traps and localized charges at the dielectric interface. These trap states introduce an additional capacitance in parallel with the channel, effectively screening the gate and slowing the current rise. Thus, SS provides a sensitive probe of interface quality, with lower values indicating cleaner and more abrupt switching.

Beyond switching sharpness, the ease with which carriers move through the channel is described by the field-effect mobility (μ_{FE}), following the equation **Equation 13**:

$$\mu_{FE} = \frac{L}{WC_{OX}V_{DS}}g_m \quad \textbf{Equation 13}$$

Where g_m is the transconductance, which quantifies how effectively the drain current responds to changes in the gate voltage. In other words, it measures the sensitivity of channel conduction to electrostatic control by the gate and can be described as in **Equation 14**:

$$g_m = \frac{dI_{DS}}{dV_{GS}} \quad \textbf{Equation 14}$$

μ_{FE} reflects both the intrinsic scattering in the 2D lattice and the extrinsic influence of the dielectric environment and contact resistance. Field effect mobility remains a crucial indicator of how device processing and interface engineering affect charge transport in practical devices.

The role of the contacts is directly expressed through the contact resistance (R_c), which quantifies the additional series resistance arising from carrier injection across the metal/2D interface. R_c tends to be relatively high and strongly dependent on contact geometry. If the

physical overlap length of the contact is shorter than the transfer length - the characteristic distance carriers require to spread laterally into the channel - current crowding occurs and R_C rises sharply. The effective resistance of the 2D sheet itself also plays a role: the sheet resistance (R_{sh}), defined per square, depends on the carrier density and thickness of the channel, with thinner or less doped layers exhibiting larger R_{sh}. Together, R_c and R_{sh} determine how efficiently the intrinsic mobility of the channel can translate into actual current in a device.

From an electrostatic perspective, the total charge Q_g induced in the channel is directly governed by the gate voltage V_G. For a dielectric layer of thickness t_d and relative permittivity κ, the capacitance per unit area is described by the equation **Equation 15**:

$$Q_g = V_G \frac{\kappa \epsilon_0 A}{t_d} \qquad \textbf{Equation 15}$$

where ε_0 is the vacuum permittivity. Because different dielectric materials possess different permittivities, it is often useful to compare them through the concept of equivalent oxide thickness (EOT). The EOT maps any dielectric to the thickness of SiO_2 that would yield the same capacitance, and is given by **Equation 16**:

$$EOT = t_d \frac{\kappa_{SiO2}}{\kappa_d} \qquad \textbf{Equation 16}$$

This normalization highlights the benefit of high-κ dielectrics: for the same physical thickness, materials such as HfO_2 or Al_2O_3 provide a much larger C_g than SiO_2, enabling stronger electrostatic coupling to the 2D channel without increasing leakage currents. In practice, this allows the fabrication of transistors with reduced EOT and therefore tighter gate control, while maintaining a physically thicker oxide layer that improves reliability against tunneling breakdown. However, realizing these advantages in 2D FETs is complicated by the inert, dangling-bond-free nature of van der Waals surfaces, which makes uniform nucleation of high-κ oxides challenging and often necessitates additional interface engineering steps.

Finally, non-idealities in the dielectric and its interface with the 2D semiconductor manifest as hysteresis in the transfer characteristics. This hysteresis, typically measured as a shift in the apparent threshold voltage between forward and reverse gate sweeps, arises from charge trapping and detrapping dynamics. Its magnitude depends on the density and energy distribution of traps, as well as on the sweep rate and voltage range. Minimizing hysteresis, therefore requires not only the selection of high-κ dielectrics with stable permittivity across frequency,

but also careful engineering of clean, trap-free interfaces that preserve the intrinsic electrostatics of the 2D channel.

2.3. Contact resistance and gate dielectric interface challenges

As discussed earlier, there are numerous challenges in realizing reliable FETs based on 2D materials. In this manuscript, I will concentrate on two key challenges that hinder the performance of 2D material FETs: (1) achieving low-resistance contacts between metal electrodes and the 2D semiconductor, and (2) integrating high-κ gate dielectrics on the inert surface of 2D semiconductors. These issues arise from the unique physics of 2D materials and have prompted extensive research into innovative engineering solutions

2.3.1. Contact resistance in 2D FETs

Unlike bulk semiconductors, where heavily doped source/drain regions yield ohmic contacts, 2D semiconductors cannot be easily doped, and their metal contacts often form Schottky barriers. In the ideal Schottky-Mott limit (neglecting interface effects), the n-type barrier height is expressed by **Equation 2**. Fermi-level pinning at the metal/2D interface, however, causes the actual barrier to deviate from this ideal. In practice, the Fermi level tends to be pinned at a nearly fixed energy in the bandgap, making the barrier height relatively insensitive to the metal's work function. The strength of this pinning is quantified by a pinning factor (**Equation 17**):

$$\boldsymbol{S = \frac{d\Phi_B}{d\Phi_M}} \qquad \textbf{Equation 17}$$

Pinning factor is a measure of how strongly the Fermi level at the metal-semiconductor contact follows the metal work function. The Schottky barrier heights in the presence of pinning can then be expressed as in **Equation 18** and **Equation 19** for electrons (Φ_{Bn}) and holes (Φ_{Bp}), respectively.

$$\Phi_{Bn} = S(\Phi_M - \Phi_{CNL}) + \Phi_{CNL} - \chi \qquad \textbf{Equation 18}$$

$$\Phi_{Bp} = S(\Phi_{CNL} - \Phi_M) + E_g + \chi - \Phi_{CNL} \qquad \textbf{Equation 19}$$

When S = 1, the ideal Schottky–Mott case is recovered and no FLP occurs, while for S = 0 the barrier height is fully determined by the charge neutrality level Φ_{CNL}. The charge neutrality level is the characteristic energy within the semiconductor band gap at which donor-like and

acceptor-like interface states balance; the semiconductor Fermi level is effectively pinned close to this level, regardless of the contacting metal.

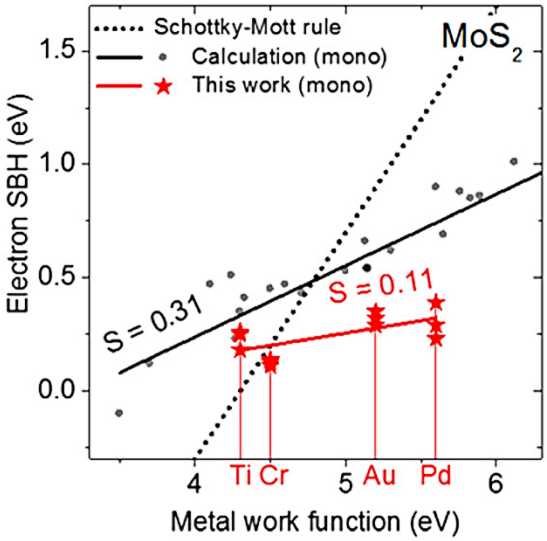

Figure 7 *Example of Fermi-level pinning in MoS_2. Schottky barrier heights (SBH) of monolayer MoS_2 plotted as a function of metal work function. The pinning factor (S) was extracted by fitting the data to the Schottky–Mott relation (dotted line). The experimentally obtained SBH values for monolayer MoS_2 are indicated by the red line, while the black line and dot represent the calculated monolayer SBH*[34].

In realistic interfaces, many aspects affect band alignment. At the metal/2D junction, metal-induced gap states (MIGS) and defect-induced gap states (DIGS) appear inside the semiconductor band gap. Experiments on monolayer MoS_2 (**Figure 7**) with various metals find S close to 0.1. It was shown that even using an extremely low-Φ_M metal (e.g. Sc, work function 3.5 eV) cannot eliminate the Schottky barrier[35]. Structural defects such as vacancies, substitutions, or extrinsic contamination, combined with strong orbital hybridization between the metal and the chalcogen atoms, generate mid-gap states that disrupt the intrinsic band structure and effectively pin the Fermi level (**Figure 8**). Simultaneously, interfacial dipoles form due to charge redistribution - originating from unsaturated bonds or metallic impurities - which alter the effective metal work function and further reinforce pinning.

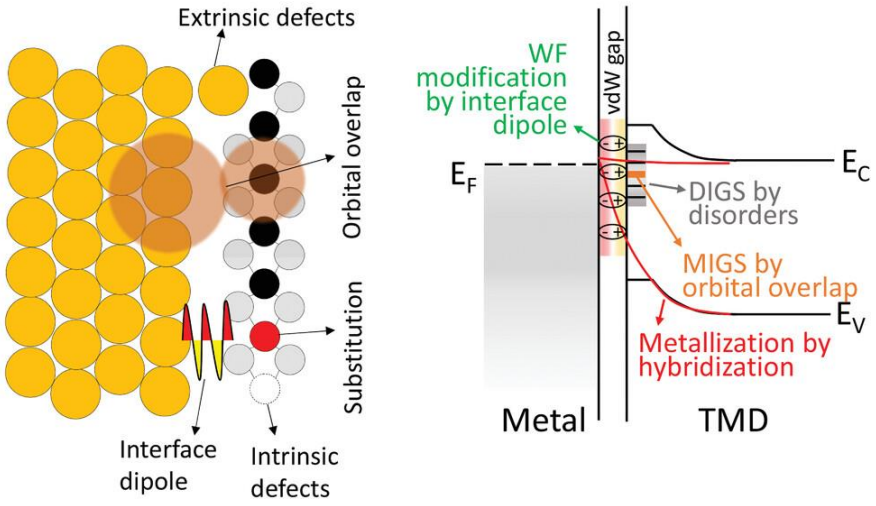

Figure 8 *Schematic and band structure of realistic contacts in 2D devices, illustrating how defects, interface dipoles, and orbital hybridization can introduce gap states and work-function modification, leading to strong Fermi-level pinning*[14].

The result is that typical contacts to 2D semiconductors show large contact resistances on the order of kΩμm, severely limiting current injection. Such high R_C in metal/2D material junctions not only curtails the ON-current but also dominates the total resistance in short-channel devices, undermining the benefits of the 2D channel's intrinsic mobility[14].

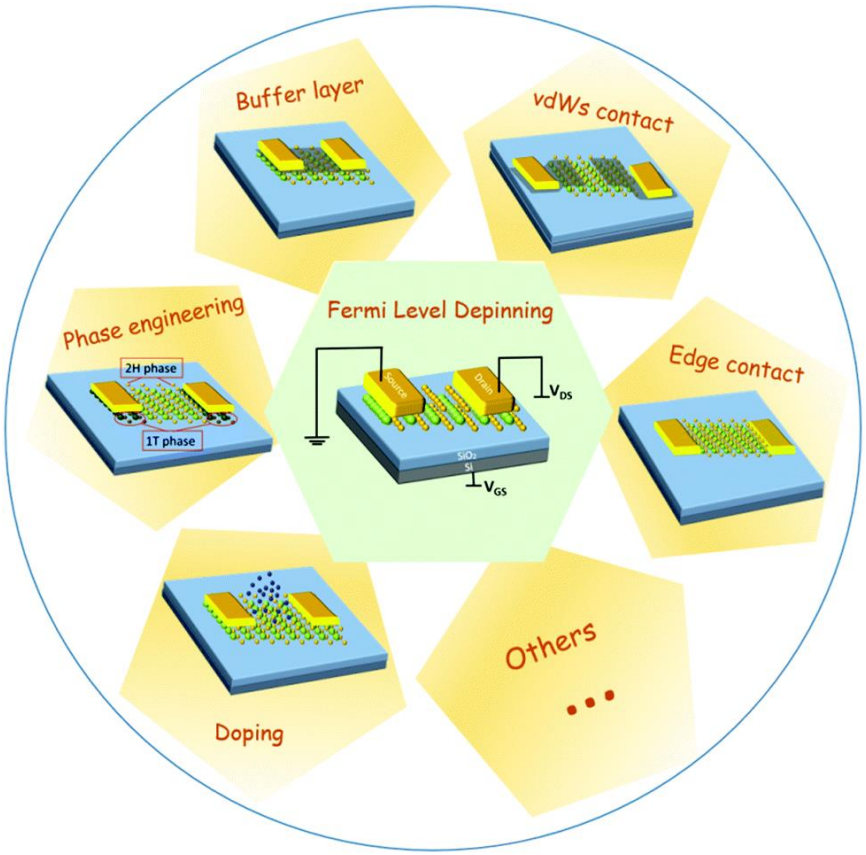

Figure 9 *Strategies for Fermi-level depinning*[36].

To mitigate this problem, a variety of depinning strategies have been developed, schematically illustrated in **Figure 9**. These include introducing ultrathin buffer layers at the metal/semiconductor interface, employing van der Waals contacts, inducing phase transitions in the semiconductor, forming edge contacts with 3D metals, and tuning the semiconductor through chemical doping[36]. Each of these approaches will be discussed in detail in the following subsections.

Buffer Layers

One of the most established approaches to mitigate Fermi-level pinning in 2D semiconductors is the insertion of an ultrathin buffer layer between the metal electrode and the active channel. The purpose of this interlayer is to decouple the semiconductor from the metal's electronic states, thereby reducing or eliminating MIGS and DIGS at the interface. By weakening direct orbital hybridization and neutralizing interface dipoles, buffer layers allow the effective barrier height to more closely follow the Schottky–Mott prediction.

Transition metal oxides have been particularly successful in this role. Oxides such as MoO_x, TiO_2, Al_2O_3, and Ta_2O_5 not only screen interface dipoles but can also induce charge transfer that locally dopes the semiconductor, thinning the Schottky barrier. For instance, MoO_x has been shown to improve hole injection in MoS_2 by reducing the effective barrier height to below 150 meV, enabling p-type conduction[37]. Similarly, thin Al_2O_3 interlayers deposited on MoS_2 significantly decrease contact resistance by both passivating defect states and providing a tunneling-mediated pathway for carriers[38].

Organic and molecular intercalation layers have also proven effective. Thiol-terminated self-assembled monolayers can bind to metal electrodes and form an ordered dipolar film at the interface[39]. Such molecular layers not only suppress gap states but also modulate the effective work function of the metal, enabling systematic tuning of the Schottky barrier height. Importantly, these layers allow the dominant transport mechanism to shift from thermionic emission over a high barrier to tunneling through a thin potential barrier, which is more efficient at the nanoscale.

Two-dimensional materials themselves are increasingly employed as buffer layers, creating van der Waals-type contacts that minimize FLP. Graphene interlayers are a prime example: when inserted between the metal and MoS_2, the graphene acts as a Fermi-level relay, with its own work function tunable by electrostatic gating or chemical doping[40]. This allows the effective Schottky barrier height at the MoS_2 channel to be adjusted, rather than locked by pinning at the

direct metal–semiconductor interface. Hexagonal boron nitride (h-BN) has also been used in this context, particularly for p-type devices, where it prevents direct orbital overlap while maintaining efficient tunneling, leading to improved hole injection into WSe_2[41]. More recently, conductive 2D materials such as MXenes have been explored as interlayers; their metallic conductivity combined with van der Waals bonding enables both strong carrier injection and reduced FLP[42].

A key design trade-off for buffer layers is their thickness. While increasing the thickness tends to suppress more interface states and further reduce the Schottky barrier height, it simultaneously increases tunneling resistance, which can counteract the benefits of depinning. Therefore, optimized interlayer thicknesses are typically on the order of one to a few nanometers, balancing depinning effectiveness with carrier injection efficiency. Nevertheless, this strategy is, in most cases, not readily scalable, as it relies on mechanically exfoliated flakes. Furthermore, the flake transfer process can introduce interfacial contamination and structural non-idealities, both of which degrade interface quality and contribute to additional contact resistance. Despite these challenges, mentioned experimental reports show that properly optimized buffer layers can reduce contact resistance by as much as 55–90%, underscoring their practical impact on device performance.

van der Waals metals

One effective strategy to suppress Fermi-level pinning is to physically avoid the interfacial damage and disorder typically introduced by conventional lithographic patterning and metal evaporation. Standard top-contact fabrication often creates DIGS at the interface due to energetic deposition or contamination during processing, which in turn enhances FLP. To overcome this, dry transfer techniques have been developed that allow pre-fabricated metal layers or patterns to be mechanically laminated onto the surface of a 2D semiconductor, forming a van der Waals-type contact without direct energetic impact on the crystal lattice.

The first demonstrations of this concept showed that embedding metal electrodes within h-BN and then transferring the entire stack onto graphene or $NbSe_2$ created atomically clean interfaces and stable electrical contacts. In these devices, contact resistances as low as ~0.1 kΩ·μm were reported for $NbSe_2$ at room temperature, while WSe_2 transistors using the same geometry exhibited high hole mobility (~195 $cm^2V^{-1}s^{-1}$) and long-term ambient stability due to the protective encapsulation[14]. Subsequent advances used polymer stamps such as PMMA/PDMS to directly transfer patterned metal contacts onto TMDs. Cross-sectional TEM confirmed that such contacts preserved an atomically flat, residue-free interface, in stark contrast to the

disordered regions observed at evaporated contacts[43]. Importantly, these transferred metal interfaces yielded pinning factors approaching unity, signifying almost complete suppression of DIGS-induced FLP.

Alternative geometries have also been realized by inverting the process: instead of transferring the metal to the semiconductor, the 2D crystal can be laminated onto pre-patterned metal electrodes, forming so-called van der Waals bottom contacts. These interfaces similarly demonstrated low pinning factors, tunable transistor polarity depending on the chosen metal work function, and compatibility with complementary logic circuits such as NAND and NOR gates[44]. Even more advanced device concepts, including nearly ideal Schottky junctions[45], have been achieved using transferred metal contact schemes.

Transferred metal contacts present a powerful approach to engineer clean, disorder-free metal/2D interfaces, effectively eliminating many of the extrinsic origins of Fermi-level pinning. While their practical implementation requires careful handling and remains less mature than conventional metallization, the approach highlights a pathway to nearly ideal Schottky barrier modulation and ultra-low-resistance contacts in 2D devices. Nevertheless, this method also faces important limitations. The transfer process itself can suffer from alignment inaccuracy and mechanical stress, especially when positioning nanoscale contact patterns, which poses challenges for reproducibility and scalability to wafer-level integration. Polymer stamps or supporting layers used during the transfer may leave behind organic residues that degrade interface quality if not properly removed. Moreover, the adhesion strength between the transferred metal and the 2D semiconductor can be weaker than that of evaporated films, potentially compromising long-term device stability and contact reliability under electrical stress or thermal cycling. Finally, the requirement of multi-step fabrication and specialized handling equipment makes the process more complex and less compatible with existing CMOS manufacturing flows, limiting its immediate technological readiness compared to standard deposition techniques.

Doping and charge injection

Enhancing the carrier density in the vicinity of the metal/semiconductor interface is a powerful means of reducing contact resistance in 2D transistors. By increasing the local electron or hole concentration, the effective Schottky barrier can be thinned or lowered through band bending, thereby facilitating tunneling-dominated transport. While substitutional doping of the 2D lattice is difficult, surface charge transfer doping and oxide-derived doping have shown success[46]. For instance, depositing sub-stoichiometric aluminum oxide (AlO_x) onto MoS_2 injects electrons

into the channel (as oxygen vacancies act as donors). This method yielded a stable n-type doping that reduced sheet resistance to ~7 kΩ/□ and contact resistance down to ~480 Ω·μm, without degrading mobility or subthreshold swing[46]. The doped devices drove currents among the highest for monolayer MoS_2 – highlighting that contact doping can significantly boost performance. Chemical treatments (e.g. NO or benzyl viologen for p- or n-doping) are also used to reduce the effective barrier at contacts[47,48]. A concern with many dopants, however, is the introduction of trap states that can impair the OFF-state; careful control (such as doping only the contact regions) is needed to preserve a high I_{ON}/I_{OFF}.

Edge contacts

In contrast to conventional surface (basal-plane) metallization, edge contacts exploit the atomic edges of 2D crystals as the active interface for carrier injection. At these edges, unsaturated bonds are naturally present, enabling the formation of direct chemical bonds with the contacting metal. This fundamental distinction provides several advantages over top contacts: the injection path is not limited by van der Waals gaps, the overlap with mid-gap defect states is minimized, and current spreading into the channel is more uniform[49,50]. As a result, edge contacts can significantly suppress Fermi-level pinning and reduce contact resistance.

Experimental studies have demonstrated that edge-contacted MoS_2 and WSe_2 transistors can achieve pinning factors close to unity (0.95-0.97), indicating nearly ideal Schottky–Mott behavior[36]. In such configurations, the Schottky barrier height becomes tunable with the choice of contact metal, a capability that is not available in basal-plane geometries due to strong FLP. Low contact resistances on the order of a few hundred Ω·μm have been reported in monolayer MoS_2 using carefully fabricated edge contacts under ultra-high vacuum conditions[51]. These improvements directly translate into higher ON-currents and enhanced switching performance, particularly in short-channel devices where contact resistance dominates.

Another key advantage of edge contacts is their compatibility with device scaling. Because the metal overlaps only the thickness of the 2D layer (rather than extending laterally along the basal plane), the contact footprint can be minimized, making this geometry particularly attractive for sub-10 nm transistors. Fabrication of edge contacts, however, poses nontrivial challenges. They typically require controlled etching or patterning of the 2D material to expose clean edges prior to metallization. Any damage or contamination introduced during this step can compromise the quality of the contact. Recent advances in encapsulation (e.g., h-BN-protected etching) and clean transfer processes have mitigated some of these difficulties, enabling reproducible and low-defect edges[52]. Alternative approaches such as selective area growth of metals into pre-

defined trenches that intersect the 2D material edges have also been proposed to achieve scalable edge-contact architectures[53].

Semimetallic contacts

Semimetals such as bismuth (Bi) and antimony (Sb) have recently emerged as highly effective electrodes for 2D semiconductors[54,55]. Their low density of states at the Fermi energy suppresses MIGS and weakens orbital hybridization with chalcogen orbitals, thereby mitigating Fermi-level pinning. This enables Schottky barrier heights to follow more closely the Schottky–Mott prediction and allows efficient carrier injection without additional buffer layers. Experimental results confirm these advantages: Bi contacts to monolayer MoS_2 achieved ultralow contact resistances of ~123 Ω·μm with nearly vanishing Schottky barriers, yielding ON-currents above 1 mA/μm[54]. Even more striking, crystalline Sb electrodes reduced the contact resistance further to ~42 Ω·μm, approaching the quantum limit, while maintaining thermal stability up to 125°C[55]. Compared to buffer layers, transferred metals, or edge contacts, the semimetallic strategy is unique in relying on the intrinsic properties of the electrode material rather than elaborate interfacial engineering. Challenges remain in reproducibility, large-scale integration, and extending this approach to the full family of 2D semiconductors, but Bi and Sb currently represent one of the most promising pathways toward overcoming Fermi-level pinning and achieving near-ideal contacts.

Although buffer layers, transferred metal contacts, doping, edge contacts, and most recently semimetallic electrodes have each delivered remarkable progress in mitigating Fermi-level pinning and lowering contact resistance in 2D FETs, no single strategy has yet matured into a universally applicable solution. Each carries its own limitations, ranging from scalability and reproducibility to reliability under realistic operating conditions. Importantly, the advent of Bi and Sb semimetallic contacts shows that contact resistances can already approach the quantum limit, with Schottky barriers reduced to nearly zero in optimized devices. This suggests that the fundamental obstacle of contact resistance is gradually being overcome, and the bottleneck is shifting toward issues of large-scale manufacturability and process integration. The critical challenge ahead is therefore not only to push R_c further downward, but to ensure that ultralow-resistance contacts can be realized reproducibly across wafer-scale device arrays in a CMOS-compatible fashion. Achieving this will require continued refinement of interface engineering and fabrication methodologies, with an emphasis on stability, yield, and compatibility with industrial process flows. These considerations set the stage for later parts of this thesis, where

the issue of contact resistance reappears in an experimental context, providing direct insight into how interlayer-based interface engineering can shape carrier injection in 2D FETs

2.3.2. *High-k dielectric integration on 2D materials*

In 2D field-effect transistors the dielectric layer plays a decisive role, as its intrinsic properties and extrinsic quality directly determine device performance. Several key aspects govern the electrostatics: the band gap of the dielectric, its dielectric constant, the presence of interface states, and the density of defects, which is schematically presented in **Figure 10**. The band gap defines the barrier height that prevents charge leakage from the channel into the gate.

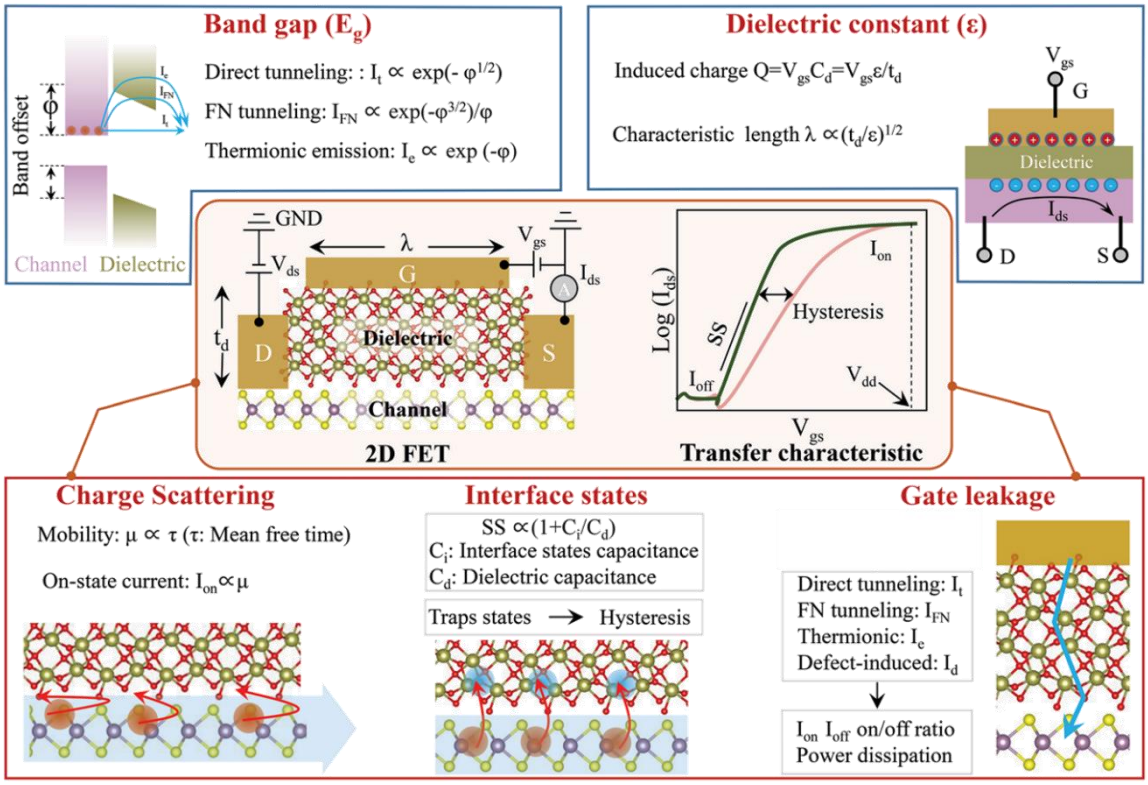

Figure 10 *Schematic representation of main aspects and phenomena that influence gate dielectric properties and govern the figures of merit in 2D FETs*[56].

A sufficiently large band gap suppresses various leakage mechanisms, including direct tunneling, Fowler–Nordheim tunneling, and thermionic emission, thereby reducing power dissipation and preserving a high I_{ON}/I_{OFF} ratio[56]. The dielectric constant (κ) controls the gate capacitance (C_g), and the induced charge can be expressed by **Equation 20**:

$$Q = V_G C_g \qquad \textbf{Equation 20}$$

A higher κ enables strong electrostatic coupling without requiring an ultrathin physical layer, which is essential for maintaining low EOT and effective gate control in scaled devices.

However, interface states at the dielectric–channel boundary introduce trap states that capture carriers, causing hysteresis in the transfer characteristics and increasing the subthreshold swing, which depends on interface states and dielectric capacitance, directly limiting the switching efficiency of the device. Additionally, charge scattering from interfacial defects and disorder reduces the carrier mobility and therefore lowers the ON-state current. Defects in the dielectric itself also provide additional leakage paths, further deteriorating device reliability.

The motivation for introducing high-κ dielectrics in the first place comes from the limitations of SiO_2 in aggressively scaled MOSFETs. As the technology node continued to scale down, maintaining strong gate control required extremely thin SiO_2 layers, on the order of 1 nm or less. At such thicknesses, quantum mechanical tunneling currents across the oxide became unacceptably large, leading to severe gate leakage and power dissipation. Replacing SiO_2 with high-κ oxides such as HfO_2 allowed the same or even larger gate capacitance to be achieved with a physically thicker insulating layer, thereby drastically suppressing tunneling while maintaining electrostatic control. Large κ combined with a sufficiently wide band gap - established high-κ oxides as the industry standard for modern CMOS.

On this foundation, the challenge of integrating high-κ dielectrics with 2D materials becomes clear. Ultra-thin transistors require high gate capacitance and low EOT, which in practice necessitates the use of high-κ oxides such as HfO_2, Al_2O_3, or ZrO_2 instead of SiO_2. These materials allow strong gate–channel coupling while mitigating tunneling leakage, and in fact top-gated MoS_2 FETs often employ 10–30 nm of HfO_2 or Al_2O_3 to enhance field-effect mobility through impurity screening and to improve the subthreshold swing by boosting gate capacitance. In state-of-the-art Si-based MOSFETs, such high-κ layers are typically integrated by ALD. During ALD, gas-phase precursors are pulsed sequentially and undergo self-limiting surface reactions, enabling atomic-scale thickness control and highly conformal coverage. This process ensures high film quality and strongly suppresses gate leakage currents. A critical requirement, however, is the presence of abundant nucleation centers on the substrate surface. Silicon surfaces naturally contain dangling bonds that act as nucleation sites, making ALD straightforward and leading to uniform dielectric layers. In contrast, 2D materials possess dangling-bond-free basal planes, which results in very low nucleation density when conventional ALD recipes are applied. As a consequence, precursors tend to nucleate only on sparse defective sites, and subsequent ALD cycles grow isolated oxide islands rather than continuous films[57]. Such discontinuous coverage severely compromises gate insulation in 2D FETs, leading to pronounced leakage currents. Conventional thermal ALD processes optimized

for silicon or 3D oxides, for example using H_2O or Al_2O_3, fail on MoS_2 or graphene, leading to patchy, island-like oxide coverage (**Figure 11**). Consequently, researchers began to focus on developing strategies to overcome this problem.

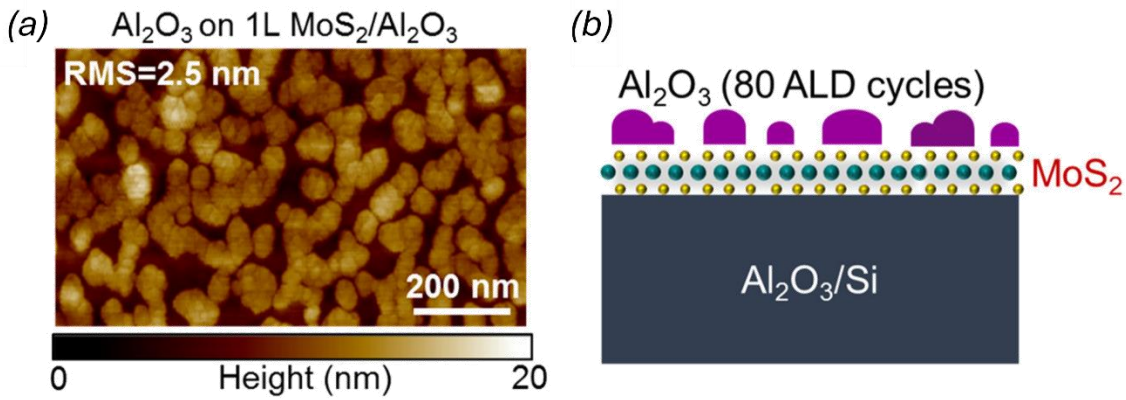

Figure 11 (a) *AFM scan and* ***(b)*** *schematic illustration of the morphology of an Al_2O_3 layer grown on the inert surface of a monolayer MoS_2. The dielectric exhibits a discontinuous, island-like surface*[57].

The state of the art follows two complementary directions: (i) adapting conventional ALD processes to 2D surfaces (activation[58], PEALD - plasma-enhanced atomic layer deposition[59,60], seeding[61,62], and selective chemical conversion[63,64]), and (ii) replacing 3D oxides with vdW-compatible dielectrics[65–67]. Below, I outline the key strategies, their physical rationales, and typical device-level outcomes, together with design rules relevant to MoS_2 n-FETs and WSe_2 p-FETs.

Surface functionalization

One major strategy to enable uniform dielectric deposition on 2D materials is surface functionalization. The idea is to activate the inert basal planes with chemical groups that can serve as anchoring sites for ALD precursors. To create nucleation sites, researchers have used chemical or plasma treatments that generate surface oxygen or defects[58]. For example, controlled ozone or UV–O_3 exposure can deposit a sacrificial oxide on MoS_2[59], enabling later uniform Al_2O_3 ALD. However, follow-on studies find that this process is highly inconsistent: excessive ozone can oxidize or damage the 2D lattice, and it is difficult to control the reaction[56,68]. Similarly, brief O_2, H_2, N_2 or Ar plasma treatments can knock out atoms or create chalcogen vacancies that serve as ALD nucleation sites. Such treatments do promote more continuous oxide films, but at the cost of creating defects. In practice these methods tend to damage the topmost 2D layers or introduce trap states that degrade mobility. Surface functionalization can locally enhance ALD nucleation, but it often leaves residues or defects on

the channel. Thus, even with aggressive pre-treatments, perfectly uniform ALD oxide growth on a pristine 2D surface remains elusive.

Plasma-enhanced and modified ALD processes

A second strategy is to modify the ALD chemistry itself so that nucleation occurs more readily on inert surfaces. In PEALD or remote-plasma ALD, reactive radicals (for example from an O_2, N_2, or H_2 plasma) are generated in situ to activate the precursors. The plasma does not directly bombard the 2D channel, but it creates highly reactive species (–OH, –N, –H etc.) that more readily adsorb on a pristine lattice. The excited precursors in PEALD can nucleate quickly even on surfaces without bonds. In practice, this has enabled some of the thinnest high-κ films on 2D materials; for example, PEALD was used to deposit ~3.5 nm of HfO_2 on MoS_2, yielding a continuous, pinhole-free film and transistors with I_{ON}/I_{OFF} ratio $>10^6$ [69]. Such results suggest that plasma-activated chemistry can overcome the nucleation barrier. Nevertheless, the high reactivity also means plasma ALD invariably creates defects. Both direct plasma pretreatment and PEALD introduce dangling bonds and disorder that degrade the atomic thin channel. It was reported that sub-3 nm HfO_2 grown by PEALD on MoS_2 inevitably damages the topmost layer[70]. In other words, although modified ALD can yield uniform high-κ films, the process tends to compromise the 2D semiconductor.

Seeding and buffer-layer approaches

An alternative strategy is to introduce an ultrathin intermediate layer on the 2D surface that provides dangling bonds or functional groups to initiate ALD. One class of seeding layers is organic molecular films. Certain molecules (for example, titanyl phthalocyanine or perylene derivatives) can physisorb on 2D materials and present functional groups to bind ALD precursors. TiOPc (titanyl phthalocyanine) on WSe_2[60] or PTCDA (3,4,9,10-perylene-tetracarboxylic dianhydride) on MoS_2[71] can serve as a nucleation template: Al_2O_3 or HfO_2 deposited on these molecular layers is continuous and uniform, with very low leakage. For instance, TiOPc monolayers on WSe_2 enable deposition of pinhole-free Al_2O_3 and greatly reduce gate leakage and hysteresis. Likewise, PTCDA films grown by van der Waals epitaxy on MoS_2 allowed growth of HfO_2 with an effective oxide thickness near 1 nm, yielding transistors with near-ideal subthreshold slopes and very high I_{ON}/I_{OFF} ratios. In these cases the organic seed provides a covalent "handle" for ALD precursors while preserving a sharp, contamination-free interface.

In parallel, ultrathin inorganic buffer layers have been explored. A common method is to evaporate ~1 nm of a metal (Al, Hf, Ti, Y, etc.) onto the 2D semiconductor and allow it to

oxidize in air or O_2. The resulting metal-oxide film is rich in surface bonds and acts as a high-κ nucleation layer. For example, an Hf metal film oxidized on MoS_2 provides an seed, on which further ALD of HfO_2/Y_2O_3 yields a compact dielectric stack with nearly ideal subthreshold slope[72]. Similarly, evaporated Si that oxidizes to SiO_2 can seed Al_2O_3 growth, giving continuous dielectrics on MoS_2 with very low leakage currents[73]. These metal-oxide seeds can dramatically improve film coverage and conformality.

However, seeding layers also introduce new limitations. Organic films generally have very low dielectric constant, so even a monolayer can reduce overall gate capacitance unless it is kept thinner than ~1 nm. Metal-oxide seeds, on the other hand, often form amorphous oxides with defects. As it was mentioned before, evaporating metals onto 2D crystals frequently damages the top atomic layers. Moreover, the metal-oxide/2D interface itself can have traps or disorder. In practice the result is that seeding layers improve ALD nucleation but at the cost of adding more interfaces and potential scattering sites. Even with ideal seeding, achieving wafer-scale, pinhole-free ALD dielectrics is extremely challenging. The dielectric stack must satisfy scaling and leakage requirements while preserving the channel, which is a demanding tradeoff.

van der Waals dielectric films

Instead of modifying ALD, another strategy is to use dielectrics that naturally form inert, dangling-bond-free interfaces with 2D semiconductors. These include layered or quasi-layered insulators that can be transferred or grown onto 2D channels. The classic example is hBN – a van der Waals crystal with a wide bandgap (6 eV)[74]. Exfoliated hBN layers on graphene or MoS_2 present atomically flat, chemically inert surfaces, resulting in clean interfaces. Graphene devices encapsulated in hBN exhibit room-temperature mobilities exceeding 10^5 $cm^2/V{\cdot}s$, nearly the intrinsic phonon limit[75]. Likewise, 2D transistors using hBN top-gates on MoS_2 show ultrahigh I_{ON}/I_{OFF} ratios and very small subthreshold slopes, evidence that hBN behaves as an ideal dielectric on 2D channels[76]. Other layered oxides and halides (for example LaOBr[77] or $MnAl_2S_4$[78]) have been explored as gate dielectrics by mechanical transfer, taking advantage of their vdW surfaces. The appeal of these vdW dielectrics is a nearly perfect interface with no dangling bonds or fixed traps. Ionic crystals with quasi-van-der-Waals surfaces represent another emerging class of insulating materials. For example, transferable membranes of crystalline $SrTiO_3$ ($\kappa>300$) have been used as gate oxides on MoS_2, yielding FETs with $I_{ON}/I_{OFF} >10^6$ and SS below 100 mV/decade[79].

In principle, vdW dielectric materials bypass ALD entirely by being integrated as whole dielectric films. Despite their advantages, vdW/transferred dielectrics face their own

limitations. Many layered insulators have relatively low κ or narrow bandgaps, which can lead to higher leakage at aggressive scaling. Moreover, mechanical transfer of exfoliated films (like hBN) is not scalable; while CVD methods are improving, large-area single-crystal growth of such dielectrics is still challenging.

Native oxidation

Oxidation of a 2D material to form its native oxide is another approach for dielectric integration. In analogy to Si to SiO_2 transition, some TMDs can be partially converted to oxides that are themselves insulating. For instance, controlled O_2-plasma treatment of $HfSe_2$ produces a uniform HfO_2 layer bound to the remaining $HfSe_2$, with an atomically sharp interface[80]. FETs with this in-situ HfO_2 dielectric show I_{ON}/I_{OFF} $\sim 10^6$ and respectable SS (~200 mV/dec). Likewise, oxidation of layered Bi_2O_2Se yields crystalline Bi_2SeO_5 on the surface, and Bi_2SeO_5/Bi_2O_2Se FETs display SS ≈75 mV/dec[63]. In these examples the oxide is formed in intimate registry with the 2D channel, giving an ideal interface. Although in-situ oxidation is a promising approach, it is not a general solution - only few 2D semiconductors form high-quality native oxides. In practice many of the resulting oxides can be amorphous or defective unless the oxidation conditions are finely tuned.

Each integration strategy – surface activation, plasma enhanced ALD, seeding layers, or vdW dielectrics – can facilitate the deposition of a high-κ film on a 2D channel, but none completely solves the fundamental issue. All these methods still contend with the basic fact that ALD on pristine 2D surfaces lacks natural nucleation sites. Surface treatments and plasma can create sites but harm the crystal; buffer layers help nucleation but add imperfect interfaces; and transferred oxides avoid ALD but are difficult to scale and may not have ideal dielectric properties. In every case, the need for uniform, pinhole-free, high-κ dielectrics with minimal impact on the channel remains a very demanding requirement. Consequently, despite the advances in these integration schemes, achieving robust ALD growth of high-κ oxides on 2D materials continues to be a major technical issue in 2D electronics. This fundamental challenge forms one of the motivations for the experimental investigations presented later, which focus on the nucleation problem and its impact on dielectric and device performance.

Chapter 3. Methods for 2D FET fabrication and electrical characterization

The challenges discussed in the previous chapter, particularly those associated with contact resistance, dielectric integration, are closely linked to the complexity of the fabrication processes required to realize functional 2D FETs. The performance and reliability of such devices depend not only on the intrinsic properties of the channel materials but also on the quality of the interfaces, the precision of patterning, and the reproducibility of deposition and etching steps. In order to provide context for the experimental results presented later in this dissertation, the following chapter introduces the general methods used for the fabrication and electrical characterization of 2D-material-based transistors. These methods not only define the practical workflow for building devices but also serve as essential tools for extracting the key physical parameters - such as mobility, threshold voltage, subthreshold swing, and on/off ratio - that provide insight into how charge carriers move through the channel, how gate fields modulate conduction, and how switching behavior emerges in 2D FETs. The emphasis is placed on the principles and workflow of each technique, rather than the specific parameters employed in this work.

3.1. Overview of fabrication workflow

The fabrication of 2D FETs is a multi-step process (**Figure 12**) that combines the delicate handling of monolayer materials with advanced lithography, deposition, and etching techniques. The workflow typically begins with substrate preparation. This may involve the use of a pre-fabricated substrate, such as SiO_2/Si, which acts as a global back-gate, or fabrication of custom-designed substrate with local back-gate islands. In the latter case, fabrication starts from scratch and includes lithographic definition of gate regions, back-gate metal deposition, a lift-off process to remove excessive metal, followed by the deposition of a gate dielectric.

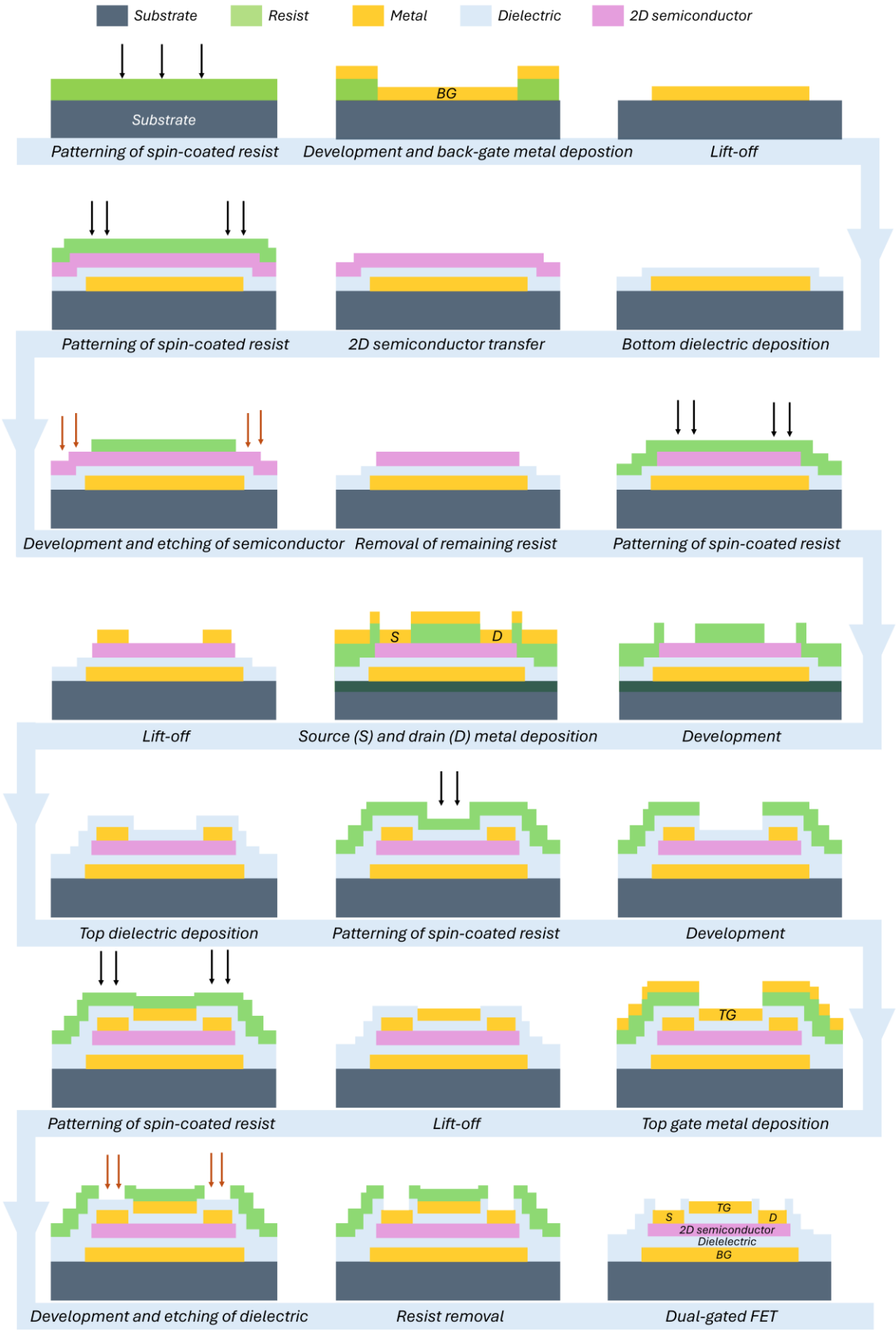

Figure 12 *A schematic summarizing the dual-gated 2D FET fabrication flow.*

Next, a semiconducting layer of a 2D material is transferred onto the prepared substrate. The channel region is then defined using a lithography technique, and unwanted material is removed by plasma etching. The fabrication of metal contacts begins with lithography to define the contact geometry, followed by metal deposition, and is finalized through a lift-off process that forms the source, drain, and probing pads.

In dual-gated device architectures, the source/drain formation is followed by the transfer or deposition of the top dielectric. Finally, the top-gate is defined using lithography, followed by metal deposition and lift-off to complete the device structure. Depending on the top dielectric thickness and coverage, an additional lithography and etching step may be necessary to open access to contact pads. This sequential and modular approach allows precise control over each component of the device architecture, enabling systematic exploration of contact and interface engineering strategies in 2D FETs.

3.2. Synthesis and fabrication of 2D materials

Through the years, a variety of techniques have been developed to obtain thin layers of 2D materials, including mechanical exfoliation[81,82], metal-organic chemical vapour deposition (MOCVD)[83,84], liquid-phase exfoliation[85,86], molecular beam epitaxy[87] and gold-assisted exfoliation[88,89]. While each method has its specific advantages depending on the target application, in this dissertation, the focus is placed on the three approaches: mechanical exfoliation, MOCVD and gold-assisted exfoliation.

Mechanical exfoliation

Mechanical exfoliation, often referred to as 'Scotch tape method', is the most widely used method for obtaining high-quality thin flakes of layered materials. It relies on the weak van der Waals bonding between adjacent layers in the bulk crystal, which allows individual atomic layers to be peeled off. In practice, a piece of adhesive tape is used to repeatedly cleave the crystal. The tape is then pressed onto the target substrate and upon removal, thin flakes - including monolayers - remain adhered to the surface. This technique provides excellent crystal quality and is widely used in research[82], but the resulting flakes are randomly distributed and vary in thickness and lateral dimensions, making the method unsuitable for scalable device fabrication.

MOCVD

MOCVD is a bottom-up thin-film deposition technique in which volatile metal-organic precursors are introduced into a high-temperature reaction chamber, where they undergo

thermal decomposition and chemical reactions to form a thin layer of the target material on the substrate surface. In the case of 2D TMDs, such as MoS_2 and WSe_2, common precursors include metal-organic compounds such as molybdenum hexacarbonyl ($Mo(CO)_6$) or tungsten hexacarbonyl ($W(CO)_6$), along with chalcogen sources such as hydrogen sulfide (H_2S) or hydrogen selenide (H_2Se)[90]. The process typically takes place at temperatures ranging from 500°C to 1000°C[91], depending on the desired material and growth conditions. During MOCVD, gas-phase precursors are transported via carrier gases (e.g., H_2, Ar) to the heated substrate surface, where surface-mediated reactions result in the nucleation and growth of crystalline monolayers.

Compared to conventional CVD using solid precursors, MOCVD offers improved control over precursor composition and flow, enabling better uniformity and reproducibility across large areas[90]. Furthermore, the use of gaseous precursors facilitates continuous and scalable processing compatible with industrial production environments.

However, MOCVD-grown films may still suffer from issues such as polycrystallinity, grain boundaries, and potential incorporation of carbon-based impurities from the decomposition of metal-organic ligands[91]. Additionally, the high cost of precursors and equipment, as well as the complexity of tuning growth parameters, can pose practical challenges.

Gold-assisted exfoliation

Gold-assisted exfoliation is a hybrid technique that combines mechanical exfoliation with surface adhesion engineering to isolate high-quality monolayers from bulk layered crystals. The process utilizes a tape coated with an ultra-smooth gold film, which is brought into contact with a freshly cleaved surface of a bulk crystal. Due to the strong interaction between gold and chalcogen atoms - stronger than the van der Waals forces holding layers in bulk together - the outermost monolayer adheres to the gold film and can be effectively separated from the parent crystal for transfer onto the desired substrate.

In contrast to conventional mechanical exfoliation, this method enables higher yield, larger flake sizes (often exceeding lateral dimensions of 500 µm), and thus improved placement control[92]. A major advantage of this approach is its wide applicability across various layered materials[88]. Furthermore, monolayers can be transferred not only onto insulating substrates but also directly onto other 2D materials, facilitating the fabrication of van der Waals heterostructures - an integration pathway that remain inaccessible via CVD or MOCVD techniques for many material combinations.

While gold-assisted exfoliation is highly effective for research and prototyping, its manual operation renders it unsuitable for industrial-scale applications. Nevertheless, its reproducibility and versatility make it an ideal method for studying novel 2D materials and heterostructure architectures in academic and experimental settings.

3.3. Lithography techniques

Lithography plays a central role in the fabrication of 2D FETs, as it enables precise spatial definition of functional regions such as the channel, gate electrodes, source and drain contacts, and pads. In experimental condensed matter physics and nanoelectronics, accurate patterning at the nanometer to micrometer scale is essential for investigating size-dependent transport phenomena, interface effects, and quantum confinement in low-dimensional systems.

Two primary lithography techniques are commonly employed in the fabrication of 2D devices in this work: electron beam lithography and direct-write photolithography. Each method offers distinct advantages in terms of resolution, flexibility, and suitability for specific feature sizes.

Electron beam lithography

Electron beam lithography is a high-resolution, maskless technique that uses a focused beam of electrons to directly write patterns into an electron-sensitive resist, most commonly polymethyl methacrylate (PMMA). This method allows for the fabrication of nanostructures with feature sizes below 100 nm, making it particularly suitable for defining narrow channels, short gate lengths, and fine metal contacts in 2D FETs. Following electron exposure, the resist undergoes development, where the exposed (or unexposed, depending on the resist type) areas are selectively removed, forming a fine-resolution mask for subsequent material deposition or etching steps. The key advantage of electron beam lithography lies in its unparalleled patterning precision and flexibility, which enables direct implementation of complex or custom-designed structures without the need for photomasks.

However, due to its point-by-point writing nature, electron beam lithography is relatively slow and has limited throughput, which can be a constraint when large areas or many devices are required. Furthermore, proximity effects and local variations in exposure dose may affect the resolution and uniformity of the final pattern, necessitating careful process calibration.

Photolithography

Photolithography is another widely used method for patterning microstructures in thin-film and nanodevice fabrication. There are two main variants: traditional mask-based photolithography, which relies on a physical photomask to define the pattern, and maskless photolithography, in

which the pattern is projected directly onto the photoresist using a digitally controlled light source.

This section focuses on maskless photolithography, also known as direct-write photolithography, as it is particularly suited for research settings where flexibility and rapid iteration are required. In this approach, the exposure system selectively illuminates the resist layer using either a focused laser or a digitally modulated light source, such as a digital micromirror device. Direct-write photolithography enables patterning of features in the sub-micron to several-micron range, which is sufficient for defining elements such as bonding pads, contact extensions, and alignment markers. After exposure, the resist is developed to remove the exposed (or unexposed) regions, forming a patterned mask for downstream processing.

The method offers several advantages in a physics research context: it avoids the need for costly photomasks, allows for quick modifications to experimental layouts, and simplifies the fabrication of custom or low-volume device designs. While the resolution is generally lower than that of electron beam lithography, maskless photolithography provides a practical compromise between precision and fabrication speed.

3.4. Metal deposition

Metal deposition is a crucial step in the fabrication of devices such as 2D FETs, as it defines the source, drain, and gate electrodes that enable electrical contact and gating of the device. The quality of the metal films, their adhesion to the substrate or 2D material, and the sharpness of the metal edges strongly influence device performance, including contact resistance and electrostatic control.

Two common physical vapor deposition techniques employed for metal deposition are electron beam evaporation and resistive evaporation. Both methods involve vaporizing a metal source under high vacuum and condensing the metal atoms onto the substrate surface to form a thin, uniform film. Electron beam evaporation uses a focused electron beam to locally heat and evaporate the metal target. This method allows for high deposition rates and efficient evaporation of high-melting-point metals such as gold, palladium, or titanium. The localized heating minimizes contamination and enables better control over the film thickness and morphology[93]. Resistive evaporation, in contrast, relies on resistive heating of a metal source wire or boat. It is a simpler and less expensive technique, suitable for evaporating metals with relatively low melting points. Resistive evaporation generally provides good film quality but can suffer from less precise thickness control compared to e-beam evaporation.

Following deposition, a lift-off process is commonly used to define the metal structures. After metal deposition onto a patterned resist, the resist is dissolved, lifting off the unwanted metal and leaving behind only the metal deposited directly on the exposed substrate in the desired device geometry.

In the context of 2D materials, the deposition of metal layers - whether for electrical contacts or gate electrodes - must be performed with particular care. Due to their atomically thin and chemically inert surfaces, 2D semiconductors are highly sensitive to metal deposition processes. During evaporation, metal atoms arrive at the substrate with relatively high kinetic energies, which can lead to physical damage, sputtering of chalcogen atoms, or creation of defects at the interface[94]. These defects may act as charge traps or scattering centers, degrading device performance and complicating charge injection. Furthermore, interface states introduced during deposition can contribute to Fermi level pinning, limiting the effectiveness of work function engineering. Process conditions such as deposition rate, chamber pressure, and substrate temperature must therefore be carefully controlled to preserve the integrity of the 2D layer and ensure clean, uniform metal coverage.

3.5. Dielectric deposition

ALD is the technique of choice for depositing gate dielectrics (most often HfO_2 and Al_2O_3) in 2D FETs due to its excellent conformality, atomic-scale thickness control, and compatibility with industrial semiconductor processing. Its self-limiting surface reactions allow for uniform coverage even on complex geometries and nanoscale features, making it ideal for ultrathin gate stacks. However, ALD on 2D materials poses significant challenges related to the lack of out-of-plane bonds and the resulting chemically inert surfaces, which impede nucleation[95]. As already discussed in previous chapter this often results in poor film uniformity and island-like growth. While ALD nucleation on pristine 2D semiconductors is problematic, this limitation does not apply when depositing on metallic layers. Metal surfaces readily support ALD growth due to the available reaction sites. As such, bottom-gate stacks that utilize ALD dielectrics deposited on metal gate electrodes do not suffer from the same nucleation issues, making ALD a robust solution for scalable fabrication of local back-gated devices. In contrast, top-gate dielectric integration on 2D channels often requires additional surface functionalization steps (e.g., ozone or plasma treatments), buffer layers, or seeding techniques to enable conformal dielectric coverage as it was mentioned before[17]. While ALD remains a highly scalable and precise method for dielectric integration, its application to 2D material interfaces requires careful surface engineering to overcome fundamental nucleation barriers.

3.6. Plasma etching

Plasma etching is a critical step in the fabrication of 2D FETs, used to define device geometries by removing unwanted portions of 2D materials or dielectric layers. Among various plasma-based techniques, reactive ion etching (RIE) is the most commonly employed due to its directional etch profile, tunability, and compatibility with standard lithographic workflows.

In RIE, reactive species are generated in a low-pressure plasma chamber by applying radio-frequency (RF) power to a selected gas mixture. These species interact with the surface through a combination of physical sputtering and chemical reactions, enabling anisotropic material removal with high precision. Parameters such as gas chemistry, chamber pressure, RF power, and etch time can be adjusted to achieve desired etch rates, selectivity, and interface quality.

For etching 2D materials such as MoS_2 or WS_2, fluorine-based chemistries - e.g., SF_6, CHF_3, or CF_4 - are commonly used, often in combination with Ar or O_2[96,97]. Fluorine radicals chemically react with metal and chalcogen atoms, breaking M–X bonds (where M = Mo, W; X = S, Se) and forming volatile by-products that are removed from the surface. Oxygen can enhance etching efficiency, particularly by facilitating chalcogen removal or cleaning residual organic materials.

In addition to etching semiconducting 2D layers, plasma processes are also used to pattern dielectric materials. For example, after top-gate dielectric deposition via ALD, it is often necessary to selectively etch high-κ oxides like HfO_2 to expose metal contact pads. In such cases, a BCl_3/Cl_2 gas mixture is typically employed. Chlorine-based plasmas are effective at breaking metal–oxygen bonds in metal oxides, forming volatile metal chlorides, while BCl_3 helps to passivate the surface and reduce surface charging[98,99]. This combination enables controlled etching of dense, stable oxides with minimal physical damage and good selectivity with respect to underlying metal layers.

While RIE is a powerful and versatile technique, care must be taken to avoid damage to the fragile monolayer materials. Excessive ion bombardment can introduce defects or degrade electronic properties. Therefore, low-power recipes, shorter etch times, and optimized gas mixtures are commonly used when processing 2D semiconductors.

3.7. Electrical characterization

Electrical characterization is essential for evaluating the performance and reliability of 2D FETs. It provides insight into carrier transport, gate control, dielectric integrity, and the impact

of contact resistance. Measurements are typically conducted using manual or automated probe stations in combination with precision source-measure units (SMUs), inductance–capacitance–resistance (LCR) meters, or semiconductor parameter analyzers.

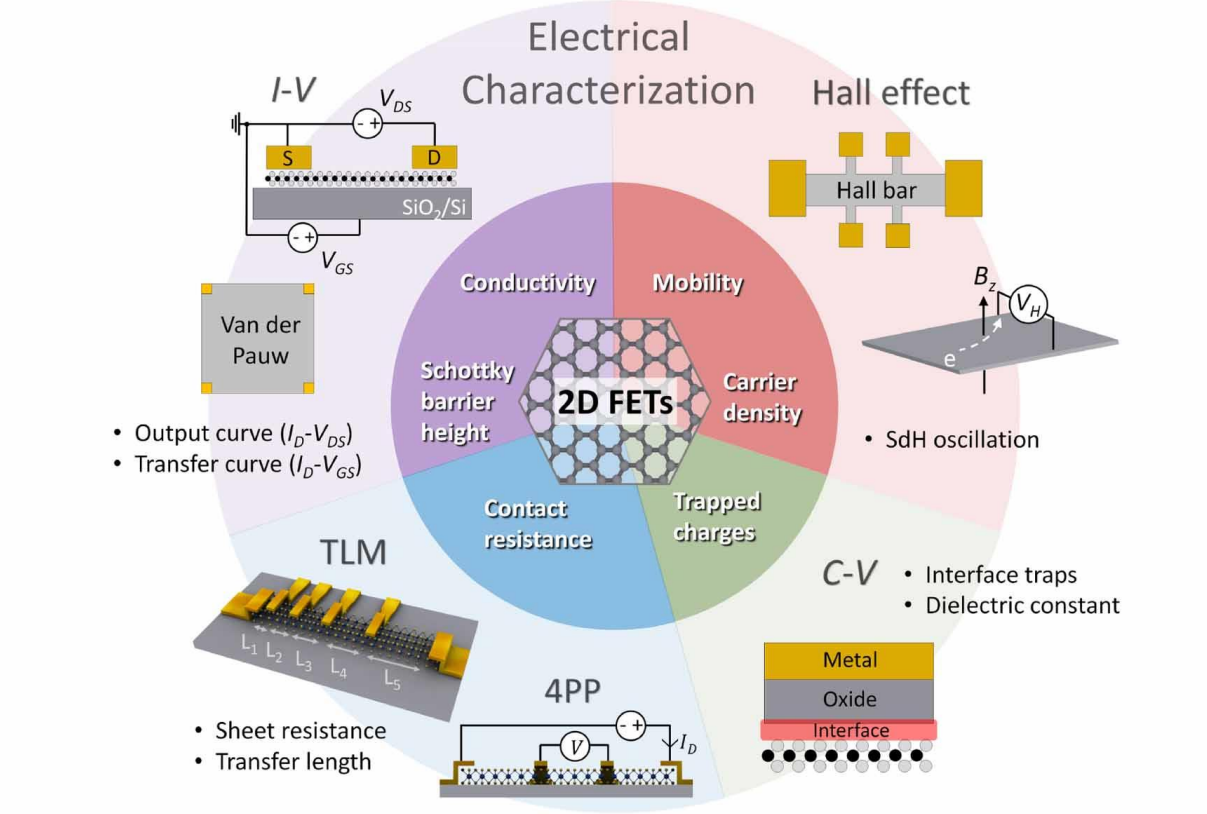

Figure 13 *Key electrical parameters of 2D FETs and the characterization techniques used to extract them. Representative quantities such as conductivity, carrier density, mobility, Schottky barrier height (SBH), contact resistance, and trapped charges can be determined through methods including current–voltage (I–V), Hall effect, capacitance–voltage (C–V), four-point probe (4PP), and transmission line method (TLM) measurements*[100].

The key electrical measurements include a range of techniques (**Figure 13**) that probe different aspects of device operation. The most common are current–voltage measurements, which provide access to conductivity, threshold voltage, subthreshold swing, and overall switching behavior. Capacitance–voltage measurements are used to extract parameters such as carrier concentration, trapped charges, and dielectric properties. Hall effect measurements enable the direct determination of carrier type, concentration, and mobility, while four-point probe techniques eliminate contact resistance to yield accurate sheet resistance values. The transmission line method is widely employed to quantify contact resistance at the metal/semiconductor interface. Together, these approaches form the standard toolkit for assessing the performance and reliability of 2D FETs. In this dissertation, the specific

measurement techniques applied to fabricated devices will be described in detail in the following subsections.

Transfer and output characteristics (I_{DS}–V_{GS} and I_{DS}–V_{DS})

Transfer characteristics (I_{DS}–V_{GS}) are recorded by sweeping the gate voltage at a fixed drain bias (**Figure 4b**) to extract key transistor parameters such as threshold voltage, subthreshold swing, ON/OFF current ratio, and field-effect mobility. In practice, the ON current is usually taken as the maximum drain current observed within the accessible gate voltage range, while the OFF current is defined either as the minimum current in the sweep or, in some cases, as the average current in the subthreshold regime to mitigate noise. The ON/OFF ratio is then determined as the ratio of these two values, typically spanning several orders of magnitude for high-quality devices.

The subthreshold swing is extracted from the slope of the transfer curve in the exponential regime, where at least two decades of current change are used for reliable fitting. Field-effect mobility is often calculated from the maximum transconductance, according to **Equation 13**. This choice ensures that mobility is evaluated in the regime of the strongest channel response. In devices with specially designed architectures featuring channels of different lengths, these measurements can also be used to extract contact resistance through the transfer length method (TLM), by analyzing the total resistance as a function of channel length.

Output characteristics (I_{DS}–V_{DS}) (**Figure 4c,d**), measured at fixed gate voltages, provide complementary insight into current saturation behavior, contact linearity, and channel modulation. The linearity of I_{DS}–V_{DS} near zero bias is often used as a qualitative indicator of contact resistance, with strongly Schottky-limited devices exhibiting non-linear output curves at low V_{DS}.

Transmission Line Method (TLM)

TLM is a widely used technique to quantitatively extract contact resistance and sheet resistance in FETs. The approach requires the fabrication of a set of test structures with identical channel widths but varying channel lengths (**Figure 14a**). By measuring the total resistance R_{tot} of each device at a fixed gate overdrive, one can analyze the linear dependence of R_{tot} on L according to **Equation 21**:

$$R_{tot} = 2R_c + R_{sh}\frac{L}{W} \qquad \textbf{Equation 21}$$

In this expression, the y-intercept of the linear fit yields twice the contact resistance, while the slope provides the sheet resistance (**Figure 14b**). The extraction is most reliable when a sufficiently wide range of channel lengths is included, typically from tens of nanometers to several micrometers, ensuring that both the contact-limited and channel-limited transport regimes are captured.

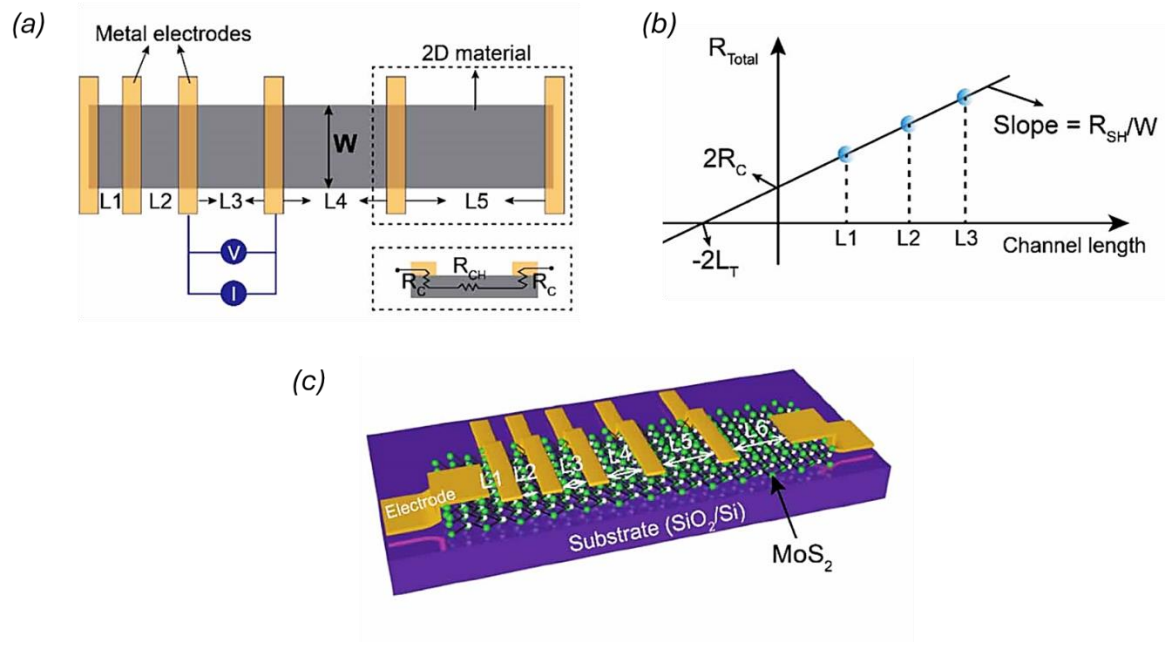

Figure 14 (a) *Top-view image of the TLM layout with channels of varying lengths. The inset highlights how the total resistance is separated into contact resistance (R_c) and channel resistance (R_{ch}), where R_{ch} is equal to $R_{sh}L/W$.* ***(b)*** *Linear fitting of the total resistance (R_{tot}) as a function of channel length, enabling extraction of R_c and the sheet resistance R_{sh}.* ***(c)*** *Schematic illustration of a MoS_2 TLM structure*[101].

Because TLM requires additional device geometries(**Figure 14c**), it is often performed on dedicated test arrays fabricated alongside the main transistors. Special care must be taken to ensure consistent contact fabrication across all channel lengths; otherwise, process-induced variability can obscure the true scaling behavior.

Capacitance measurements

Capacitance measurements are commonly used to evaluate the electrical quality of gate dielectrics, including their uniformity and potential interface trap densities. In the context of 2D device fabrication, these measurements are typically performed on separate test structures - most often metal–insulator–metal (MIM) capacitors (**Figure 15a**) - rather than directly on the FETs.

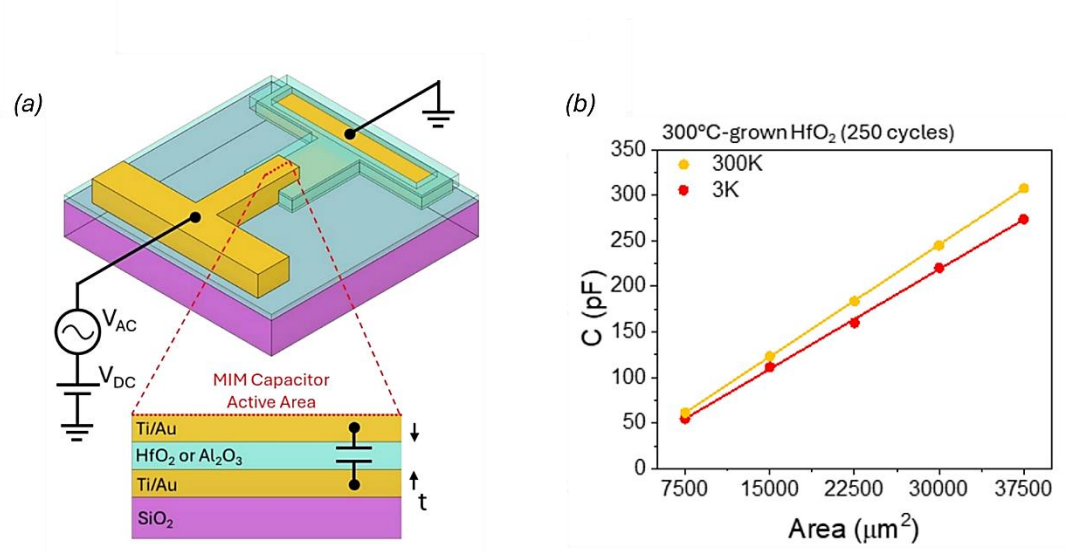

Figure 15 (a) *Schematic of a Metal-Insulator-Metal capacitor.* ***(b)*** *Example plot of capacitance versus capacitor area, used to extract the effective dielectric constant*[102].

Such structures are fabricated alongside the transistors using identical dielectric deposition conditions, allowing for a more controlled and accurate assessment of dielectric properties without the influence of the semiconducting channel.

In this dissertation, the focus was placed not on capacitance–voltage sweeps, but rather on evaluating the dependence of capacitance (C) on the capacitor area (A) at a fixed bias following the **Equation 22**:

$$C = \frac{\kappa_{eff}\epsilon_0}{d}A \qquad \textbf{Equation 22}$$

This method enables the extraction of the effective dielectric constant (k_{eff}) from the linear scaling of C with A (**Figure 15b**), offering a direct measure of dielectric performance in the integrated stack. Complementary frequency-dependent measurements can enable assessment of dielectric stability and possible trap-related dispersion. MIM-based capacitance analysis is essential for benchmarking dielectric quality and for verifying consistency across the wafer or chip.

Gate leakage and dielectric breakdown

Breakdown measurements assess the reliability of the gate dielectric. This is done by gradually ramping the voltage while monitoring the leakage current. A sudden increase in current marks the dielectric breakdown. Similar to capacitance measurements, this analysis is frequently performed on MIM structures (**Figure 15a**) to isolate dielectric behavior from semiconducting effects. The breakdown voltage is typically normalized to the dielectric thickness to obtain the breakdown field. In transistor configurations, the measurement is often expressed as a function

of the applied gate bias, since leakage and breakdown critically impact device operation. Weibull statistical analysis of breakdown voltages across a device population provides information on the distribution of failure events, allowing the extraction of characteristic breakdown strength and defect-related failure rates. Reliable dielectrics are therefore expected to combine low gate leakage at operating voltages with high breakdown fields.

Device-to-device variation and statistical analysis

Due to the sensitivity of 2D materials to fabrication conditions, environmental exposure, and intrinsic variability in flake thickness and quality, electrical performance can vary significantly between nominally identical devices. As a result, single-device measurements may not accurately represent overall material or process behavior. To obtain a realistic and statistically robust picture of device performance, it is essential to characterize a large number of devices and perform statistical analysis. Typical practice involves extracting distributions of mobility, threshold voltage, SS, and ON/OFF ratio, then representing them with histograms or cumulative plots. From these, mean values and standard deviations are reported. Such statistical benchmarking is crucial for evaluating scalability and for comparing fabrication runs. This approach enables the extraction of meaningful trends, identification of outliers, and evaluation of fabrication reproducibility - especially important in research targeting scalable and reliable 2D electronics.

The characterization practices and extraction methods described in this chapter form the experimental foundation for the work presented in the following parts of this dissertation. In particular, the subsequent three chapters apply these fabrication and measurement procedures to the investigation of 2D FETs carried out in the course of this doctoral research, unless stated otherwise.

Chapter 4. Large-area gold-assisted exfoliation of TMDs monolayers for complementary 2D FETs

This chapter is based on the publication: Giza et al., 'Exploring the Application of Gold-Assisted Exfoliation in Large-scale Integration of n-Type and p-Type 2D-FETs,' *Small Methods* 2025, 2500559. DOI: 10.1002/smtd.202500559, in which I am the first author.

4.1. Limitation of conventional exfoliation and CVD growth

Conventional methods for obtaining two-dimensional materials - mechanical exfoliation, CVD, MOCVD - each present fundamental limitations for reproducible, large-scale 2D transistor research. The standard Scotch-tape exfoliation technique produces small flakes, typically <10 μm in size, located randomly across the substrate. Their thickness, crystallinity, and local strain vary unpredictably, making systematic studies of size-dependent transport, contact resistance, and other device parameters challenging. Moreover, the uncontrolled spatial distribution of flakes complicates alignment with pre-patterned electrodes (e.g., local back-gate islands), limiting the scalability of device fabrication. On the other hand, wafer-scale CVD and MOCVD growth methods yield continuous films, but these are often polycrystalline, containing grain boundaries and defects that degrade carrier mobility, introduce local electronic inhomogeneity, and can pin the Fermi level at interfaces[103,104]. For instance, while mechanically exfoliated MoS_2 single crystals can exhibit mobilities above 200 cm^2/Vs[3], MOCVD-grown films typically remain limited to 10–50 cm^2/Vs[105], highlighting the detrimental role of grain boundaries and defect-induced scattering. The typical grain sizes, ranging from nanometers to a few micrometers[84,106,107], hinder uniform FETs performance across large device arrays. Additionally, variability in flake thickness (monolayer versus few-layer) translates directly into bandgap shifts and inconsistent transport properties, which complicates systematic benchmarking of devices. Even recent advances in high-quality single-crystal CVD growth involve complex, high-temperature processes that remain difficult to scale, with non-uniform nucleation and imperfect thickness control[103]. From a technological perspective, the high synthesis temperatures and transfer-induced contamination pose serious obstacles for CMOS back-end integration, while non-uniform domain nucleation reduces device yield and reproducibility across large arrays.

Recently, gold-assisted exfoliation[88,92] has emerged as a promising strategy to address the drawbacks of conventional mechanical exfoliation and CVD/MOCVD growth, bridging the gap between the high crystalline quality of mechanically exfoliated flakes and the scalability of

wafer-scale synthesis by enabling larger, more spatially controlled crystals suitable for device integration.

4.2. Mechanism and process of gold-assisted exfoliation

The method of gold-assisted exfoliation takes advantage of the strong Au–chalcogen interactions, whose energies can exceed ~0.5 eV, thus overcoming the relatively weak van der Waals interactions between adjacent TMD layers (e.g., -0.34 eV for MoS_2)[92]. This energetic advantage provides the driving force that enables gold to selectively peel off monolayers from bulk crystals. This principle has been implemented in two main ways: by exfoliating the crystal directly onto a gold-coated substrate[88,89], or by using a flexible gold tape to peel off the topmost monolayer of the bulk crystal[108–110]. The latter approach is particularly well-suited for later fabrication of FETs, as it enables the exfoliated monolayer to be placed onto any desired substrate (e.g., local back-gate islands) without any additional transfer steps.

In this study, a flexible Au/PMMA/thermal release tape (TRT) stack – mentioned above as gold tape – is prepared to isolate and transfer TMD monolayers, as illustrated in **Figure 16**. In the gold-exfoliation method, careful preparation of the gold tape is essential, as its quality ultimately determines the quality of the exfoliated monolayer. The use of silicon wafers as the support for the gold film is crucial, as the absence of dangling bonds on the Si(100) surface provides an atomically flat template. To ensure maximum smoothness and to remove native oxides or contaminants, the silicon surface is often mildly plasma-cleaned before gold deposition. The evaporated gold film reproduces the Si surface topography, resulting in an Au surface with a root-mean-square roughness even below 0.3 nm. This atomically smooth interface later guarantees uniform contact of the gold surface with the TMD crystal and minimizes strain during exfoliation.

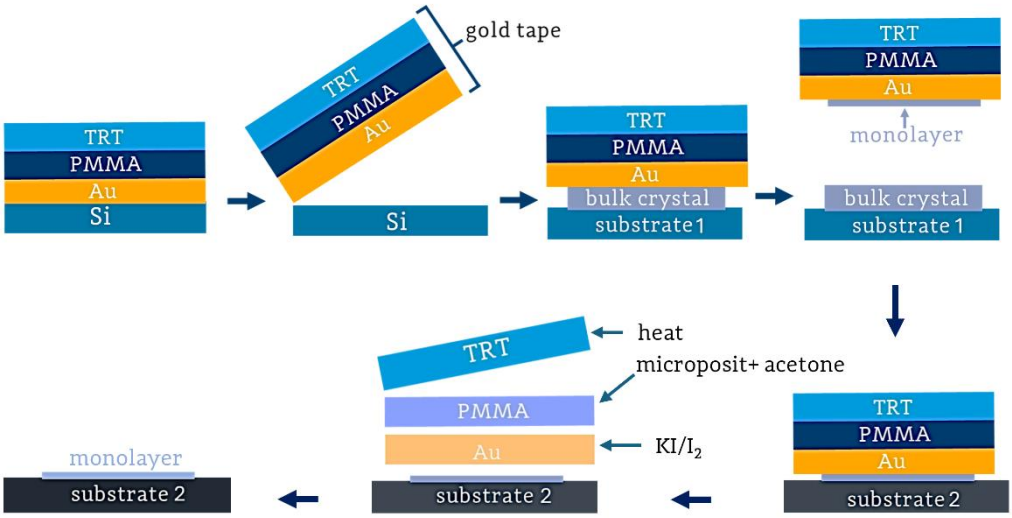

Figure 16 *Schematic of the exfoliation technique employing an Au/PMMA/TRT stack (gold tape). The gold tape is first detached from the silicon substrate and then pressed onto a bulk crystal to isolate monolayer. This monolayer is subsequently transferred onto the target substrate. After removal of all components of the gold tape, the monolayer remains attached to the substrate surface.*

The process of gold-assisted exfoliation consists of three main stages:

1. **Gold tape preparation** – A 40 nm Au film is thermally evaporated onto plasma-cleaned Si wafer, followed by spin-coating of a protective layer of 1 µm-thick PMMA and attachment of TRT. The Au/PMMA/TRT stack is then peeled off to form a flexible gold tape.

2. **Exfoliation of TMD** – The topmost layer of the bulk MoS_2 or WSe_2 crystal is first removed with scotch tape to eliminate any material that may be contaminated or oxidized. The freshly exposed surface is then brought into contact with the prepared gold tape. After applying a uniform mechanical pressure for a few seconds by pressing gently with the finger, the tape is peeled away, carrying a monolayer of the TMD bound to the Au surface.

3. **Transfer and cleaning** – The monolayer/Au/PMMA/TRT stack is aligned and placed onto the target substrate. Heating to 150 °C for 10 min improves adhesion and releases the TRT, after which the PMMA layer is dissolved in Microposit Remover (60 °C, 10 min), followed by sequential cleaning in acetone (60 °C, 10 min) and isopropanol (5 min). The Au layer is then chemically etched using a KI/I_2 solution (4 min), followed by thorough rinsing in deionized water and isopropanol to leave a clean monolayer on

the substrate. To further improve cleanliness, the sample is left in acetone for an additional 12 hours to remove any remaining residues.

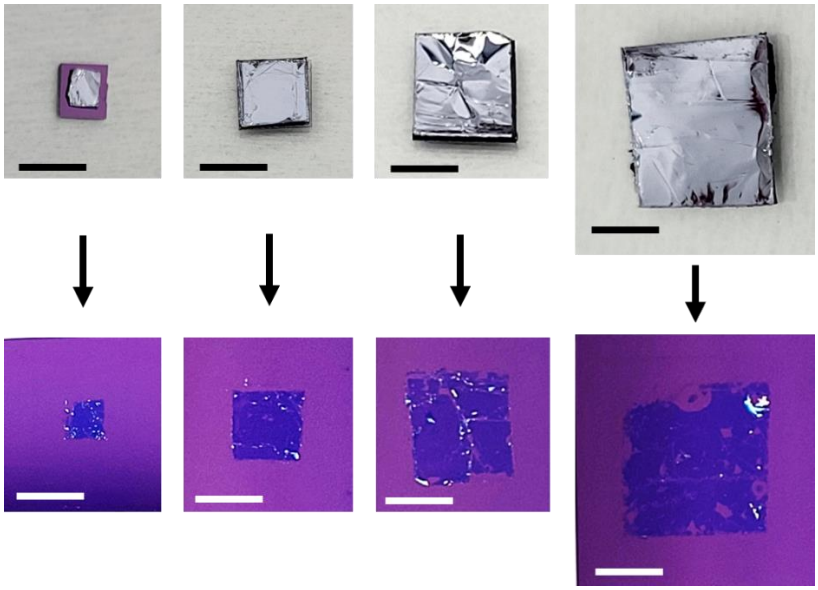

Figure 17 *Optical images of four MoS_2 bulk crystals differing in size and surface flatness, along with the respective monolayers obtained from those bulks on SiO_2/Si substrates via gold-assisted exfoliation. The white features visible on the monolayers correspond to multilayer flakes that were exfoliated together with the monolayers. Scale bars: 0.4 cm.*

The gold-assisted exfoliation method offers several key physical and technological advantages. First, it enables the preparation of large-area continuous monolayers - up to tens of square millimeters, significantly larger than typical mechanically exfoliated flakes, which are usually only tens of square micrometers in size. The monolayer dimensions are limited only by the size of the parent bulk crystal (**Figure 17**).

To investigate the uniformity and confirm the successful isolation of monolayers, Raman spectroscopy and photoluminescence (PL) were performed on MoS_2 and WSe_2 monolayers exfoliated onto SiO_2/Si substrates. Representative Raman and PL spectra are presented on **Figure 18a-d**. Both materials exhibit their characteristic Raman features together with pronounced PL emission peaks, consistent with the presence of a direct band gap in the monolayer form. For MoS_2, two separate Raman bands corresponding to the E^1_{2g} and A_{1g} modes are observed (**Figure 18a**). In contrast, the Raman spectrum of WSe_2 displays a merged E^1_{2g} and A_{1g} peak, while the B_{2g} band - commonly seen in bilayers and thicker flakes[111] - is absent (**Figure 18b**). For clarity, a bilayer spectrum is also provided, marking the position of the B_{2g} peak. In the PL spectra, both MoS_2 and WSe_2 exhibit single prominent A exciton peaks,

consistent with the direct band gap nature of these materials in the monolayer form (**Figure 18c,d**)[112].

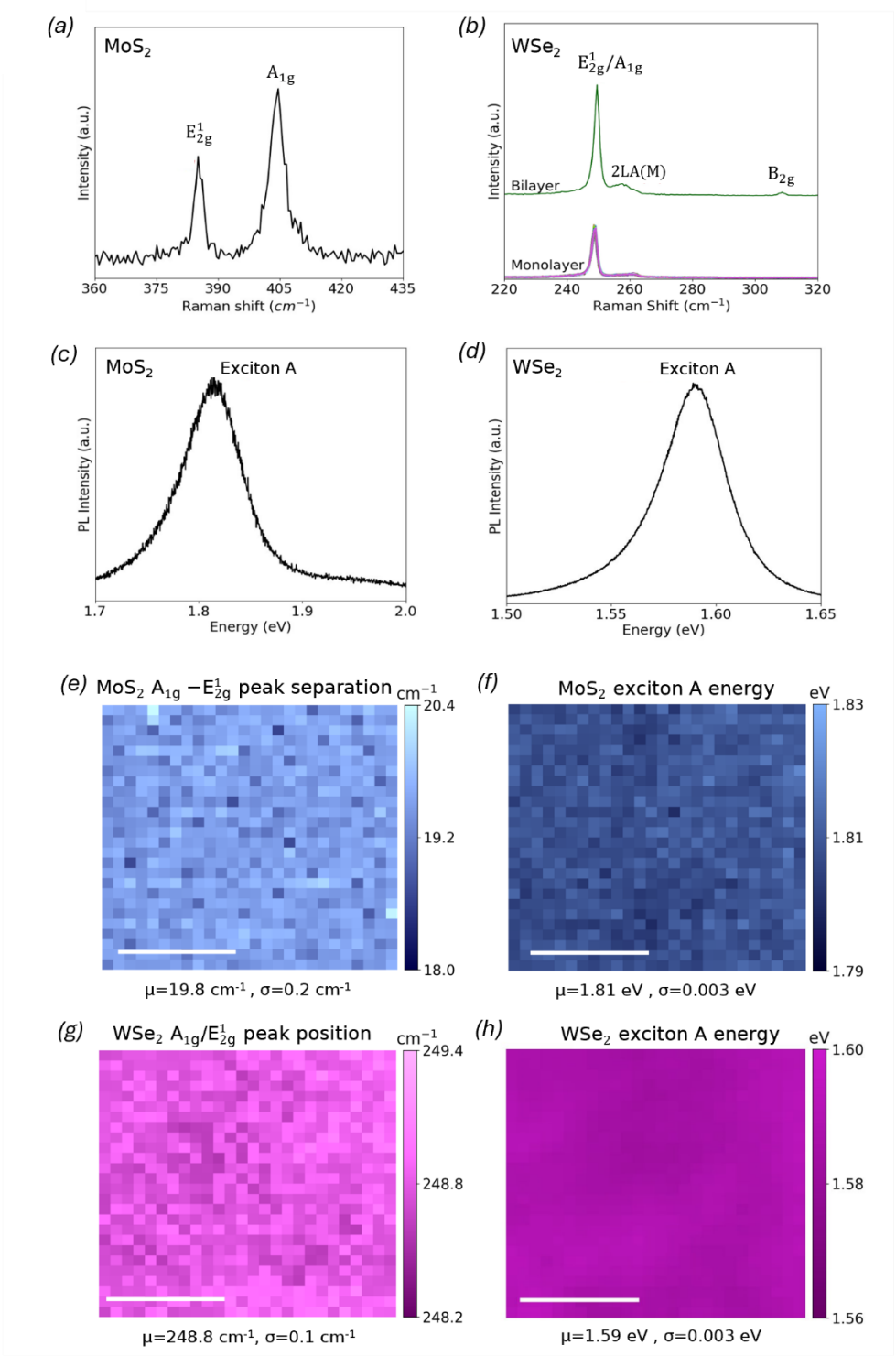

Figure 18 ***(a)*** *Raman spectrum of MoS_2 monolayers with the characteristic E^1_{2g} and A_{1g} peaks indicated.* ***(b)*** *Comparison between a representative Raman spectrum of a WSe_2 bilayer and that of a monolayer, highlighting the absence of the B_{2g} peak in the monolayer spectrum.* ***(c)*** *Photoluminescence spectrum of MoS_2 monolayers showing the position of the A exciton peak.* ***(d)*** *PL spectrum of WSe_2 monolayers indicating the A exciton peak.* ***e)*** *Raman mapping*

of the peak separation between MoS_2 A_{1g} and E^1_{2g} modes. ***f)*** *PL mapping of the A exciton energy in MoS_2.* ***g)*** *Raman mapping of the combined WSe_2 E^1_{2g} and A_{1g} peak positions.* ***h)*** *PL map of WSe_2 A exciton energy. Scale bars for all Raman and PL maps are 40 µm.*

To further assess the homogeneity, Raman and PL were also acquired in the form of spatially resolved maps. Each map was acquired over a 100 µm × 100 µm area. For MoS_2, the separation between the E_{2g} and A_{1g} Raman modes ranges from 18.6 to 20.4 cm^{-1} across the entire region (**Figure 18e**), consistent with the presence of a monolayer throughout[113–115]. The position of peaks was determined based on Lorentzian fitting. The narrow variation of this Raman mode separation highlights not only the uniform thickness but also the low local strain, which is critical for reproducible transport properties. The A exciton PL peak of MoS_2 is observed at 1.79–1.83 eV (**Figure 18f**), and its narrow energy distribution highlights the structural and compositional uniformity of the monolayer, which is critical for the consistant performance of monolayer-based devices. For WSe_2, the near-degenerate E_{2g} and A_{2g} Raman modes remain constant across the mapped area (**Figure 18g**), confirming film homogeneity. The PL mapping of WSe_2 shows the A exciton peak centered at ~1.59 eV with only minor shifts across the mapped area(**Figure 18h**), which indicates a uniform but slightly strained monolayer. Raman spectroscopy and PL measurements were conducted using Renishaw inVia Qontor Raman spectrometer with 532 nm laser, with powers of 0.34 mW for Raman and 0.034 mW for PL to minimize local heating.

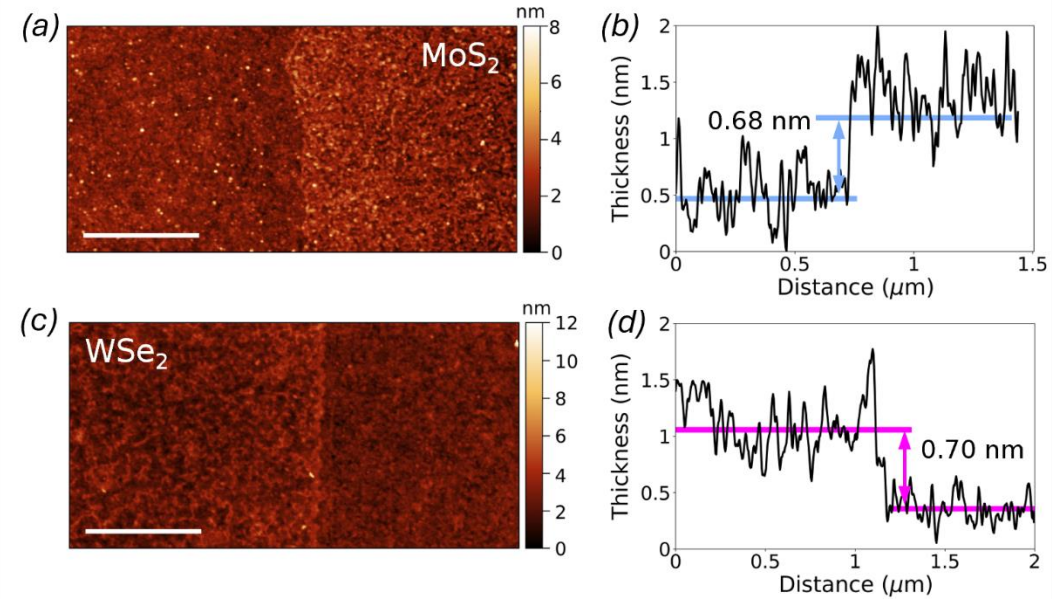

Figure 19 (a) *AFM image of MoS_2 monolayer on SiO_2/Si substrate and* ***(b)*** *corresponding thickness profile.* ***(c)*** *AFM image of WSe_2 monolayer on a SiO_2/Si substrate and* ***(d)*** *corresponding thickness profile. Scale bars are 500 nm. Measurements were performed using Bruker Dimension Icon AFM.*

AFM measurements performed over 2 μm × 1 μm regions (**Figure 19a, b**) reveal monolayer thicknesses of 0.68 nm for MoS_2 and 0.70 nm for WSe_2 (**Figure 19c, d**). These values are consistent with typical monolayer thicknesses for these materials, confirming the integrity of the exfoliation process. In addition to confirming the expected step height, AFM characterization provides additional insight into the surface morphology of the exfoliated monolayers. For WSe_2, the topography is relatively smooth and devoid of particulate features, consistent with the spectroscopic evidence of high structural uniformity. In contrast, MoS_2 surfaces display nanoscale bright spots in AFM images, which can be attributed to residual contaminants introduced during the exfoliation process. While the overall thickness across both materials remains consistent with monolayer dimensions, these localized features highlight subtle differences in surface cleanliness that may influence subsequent electrical measurements.

4.3. Performance evaluation of n-type and p-type devices made via gold-assisted exfoliation

One of the major advantages of gold-assisted exfoliation is that the monolayers are large enough to be integrated irrespective of placement, including on pre-patterned substrates, thereby enabling systematic fabrication of large device arrays. In the present study, this method yielded enough material to fabricate 120 MoS_2 (n-type) FETs and 120 WSe_2 (p-type) FETs from a single exfoliation process (**Figure 20**). The use of extended, continuous monolayers ensured that the statistical variations observed across devices were dominated by process-related factors, rather than by flake-to-flake material differences. This allowed a meaningful analysis of the intrinsic capabilities of each material in the fabricated architecture.

Both n-FET and p-FET devices were fabricated on identical local back-gated substrates. The process of substrate preparation began with electron beam lithography (Vistec Litography system) on SiO_2/Si wafers to define gate electrodes, followed by electron beam evaporation (Temescal evaporator) of a 5 nm Ti / 15 nm Pt layer, which served as back gate contact. A 10 nm HfO_2 gate dielectric was then deposited via thermal ALD. Subsequent electron beam lithography and RIE (Plasma-Therm Versalock) with BCl_3/Cl_2 plasma were employed to expose the gate pads. After gold-assisted exfoliation of the monolayers of MoS_2 and WSe_2 onto the prepared substrates, device channels were patterned by RIE using an SF_6/O_2 plasma. Finally, source–drain contacts were defined by electron beam lithography and deposited via electron beam evaporation: for n-FETs, 30 nm Au / 5 nm Ti / 30 nm Pt stack was made and for p-FETs, 10 nm Pd / 20 nm Pt to promote electron and hole transport, respectively. Moreover, the WSe_2

devices underwent an NO annealing step at 100 °C for 30 minutes to achieve p-type doping in the channels.

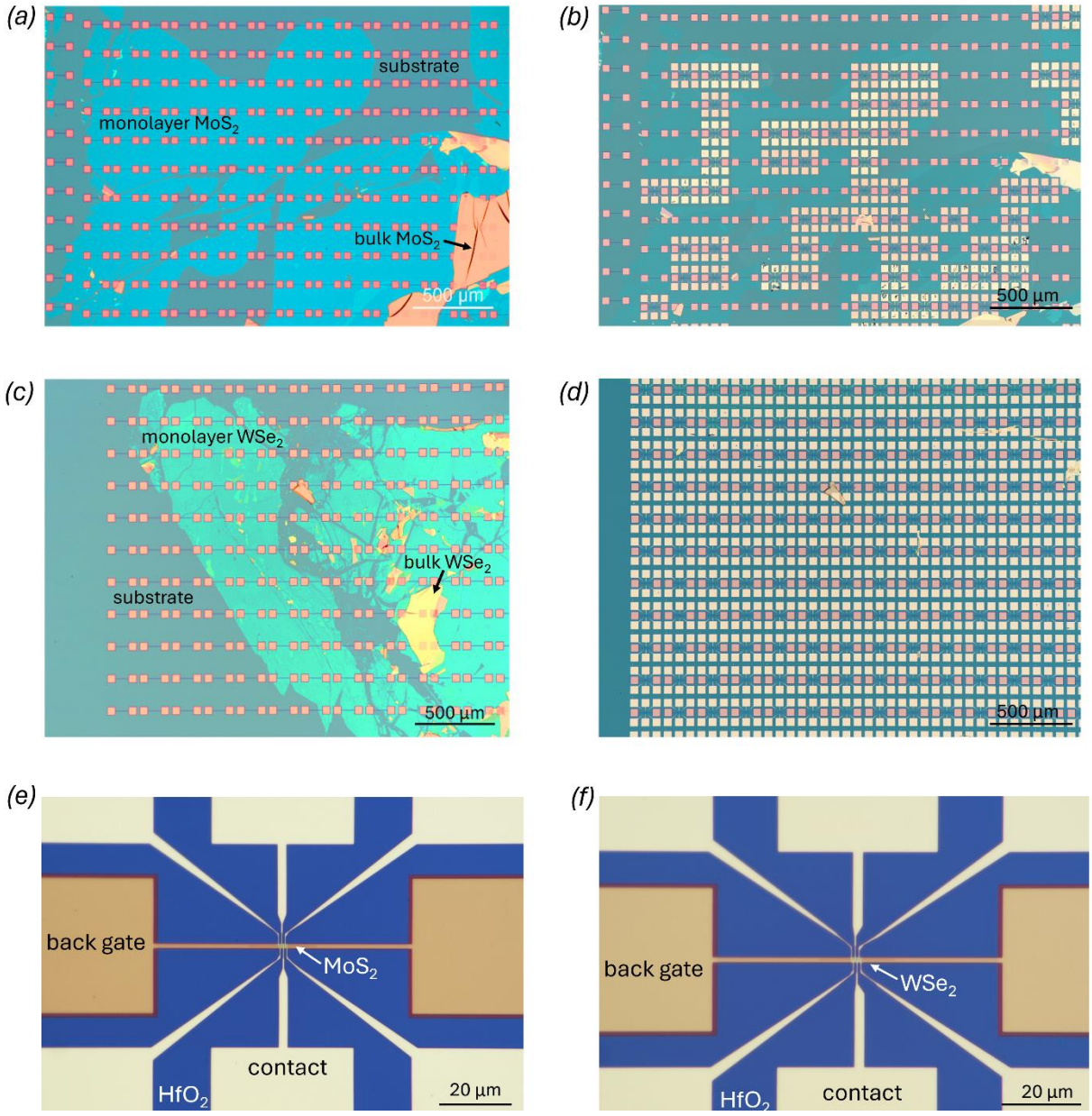

***Figure** 20 **(a)** Contrast-enhanced optical image of a large MoS_2 monolayer, exfoliated by the gold-assisted technique onto an array of pre-patterned gate islands. **(b)** The same MoS_2 region after device processing, involving channel formation through etching and subsequent metal contact deposition. **(c)** Contrast-enhanced optical image of a WSe_2 monolayer positioned on local back-gate structures. **(d)** The corresponding WSe_2 region after the fabrication of the devices. **(e)** Optical image displaying five MoS_2 devices integrated on one back-gate island. **(f)** Optical image showing five WSe_2 devices assembled on a single back-gate island.*

WSe2 p-FETs

Following fabrication, the electrical characterization was performed under ambient conditions using a probe station and Keysight B1500A parameter analyzer. Transfer characteristics measured at a drain voltage of 1 V for 120 WSe_2 p-FETs (**Figure 21a**) demonstrate remarkable uniformity. For a representative device, varying V_{DS} shows an increase in ON-state current with higher drain bias, while the OFF-state current remains stable and in the range of pA/µm, highlighting effective gate control (**Figure 21b**). Output characteristics measured at gate voltages from –1 V to –3 V exhibit a nonlinear I_{DS}-V_{DS} relationship, indicating Schottky-limited transport (**Figure 21c**). This behavior suggests that optimizing the metal–semiconductor interface could further enhance contact transparency and drive current.

Device-to-device variation was assessed by extracting key FET parameters from the transfer curves. The median threshold voltage, determined using the constant current method at 100 nA/µm, was -0.8 V with a standard deviation of 0.1 V (**Figure 21d**). This narrow distribution indicates reproducibility of the fabrication process and good uniformity of the exfoliated monolayers, which is critical for the potential use of gold-assisted exfoliation in scalable integration of 2D-material-based devices. In addition, the negative threshold voltage ensures that the WSe_2 p-FETs are switched off at $V_{BG} = 0$ V, minimizing static power consumption. The median ON-state current, measured at a carrier concentration of 1.8×10^{13} cm^{-2} (overdrive voltage $V_{OV} = 1.9$ V), was 41 µA/µm with a maximum of ~88 µA/µm and a standard deviation of 12 µA/µm (**Figure 21e**). Notably, the relatively high ON-state current confirms that gold-assisted exfoliation does not compromise the electronic quality of WSe_2 and is therefore competitive with other material preparation methods. OFF-state currents were consistently low, resulting in a high median I_{ON}/I_{OFF} ratio of 5.6×10^7 with a standard deviation of 2×10^7 (**Figure 21f**). This high switching ratio underscores the suitability of these devices for logic applications where low standby power consumption is essential, which is further discussed in the following subsection (*Comparative interpretation*).

Subthreshold slopes were sharp, with a median of 107 mV/dec and a minimum of 85 mV/dec (**Figure 21g**), indicating relatively low interface trap densities at the WSe_2/HfO_2 interface. The median field-effect mobility, calculated using the peak transconductance (**Equation 13**) method, was 6.8 cm^2/Vs with a maximum of ~14 cm^2/Vs and a standard deviation of 1.8 cm^2/Vs (**Figure 21h**). Although the median mobility is moderate, the observed maximum suggests that further optimization of interfaces and processing could improve electrical performance. It is also worth noting that mobility values reported here may be limited by contact resistance, as

suggested by the Schottky-type output characteristics (**Figure 21c**), implying that advanced contact engineering could yield further improvements.

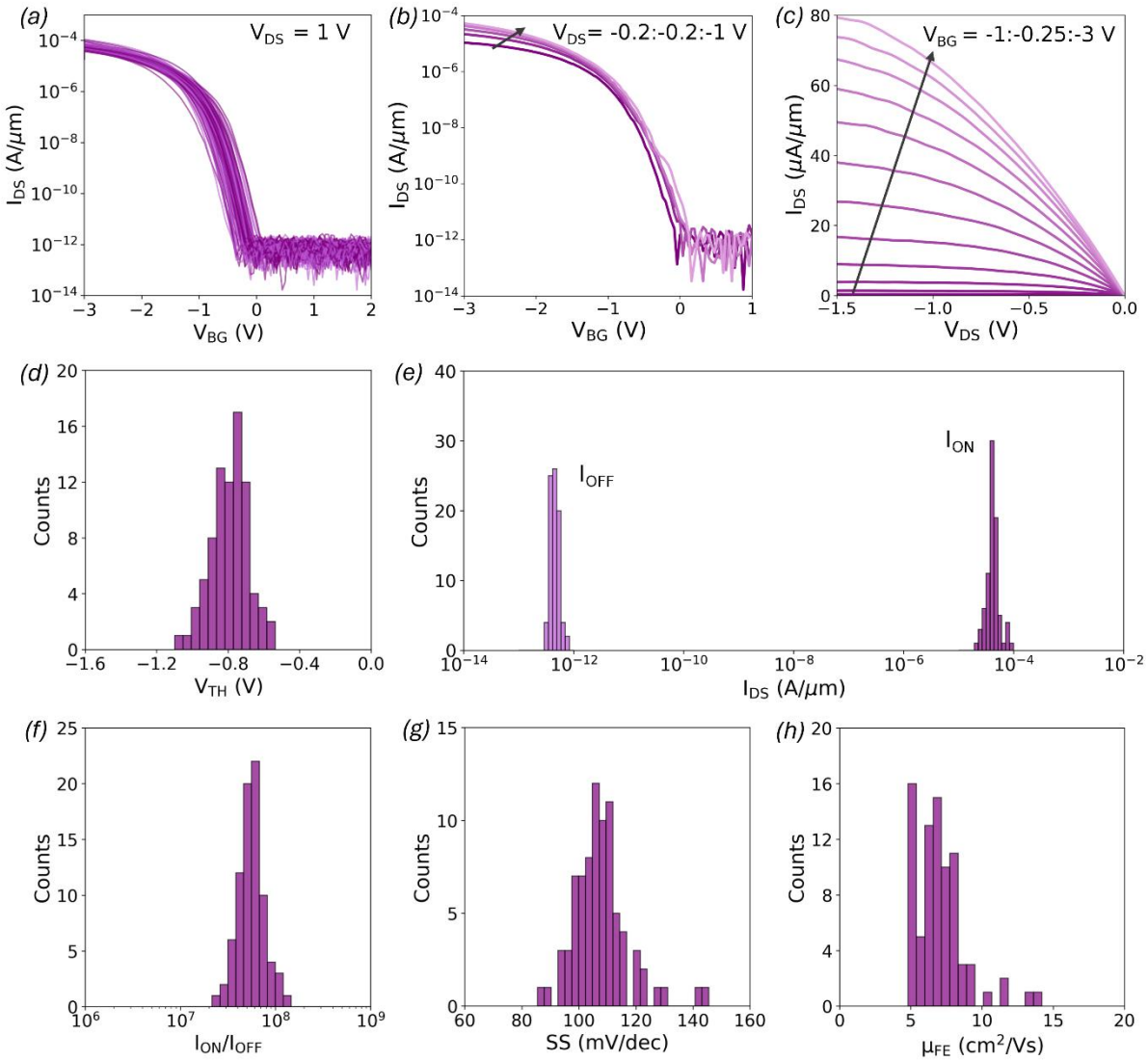

Figure 21 *Transfer curves of* ***(a)*** *120 WSe_2 p-FETs recorded at a V_{DS} of 1 V and* ***(b)*** *a representative p-FET measured with V_{DS} swept from -0.2 V to -1 V with -0.2 V step.* ***(c)*** *Output characteristics of representative p-FET obtained with V_{BG} values between -1 V to -3 V in steps of -0.25 V. Statistical distribution of* ***(d)*** *threshold voltage V_{TH},* ***e)*** *ON- and OFF-state currents,* ***(f)*** *I_{ON}/I_{OFF} ratios,* ***(g)*** *subthreshold slopes (SS) and* ***(h)*** *field-effect mobilities (μ_{FE}).*

Importantly, these are the first monolayer WSe_2 p-FETs fabricated using gold-assisted exfoliation, demonstrating the method's effectiveness in producing uniform, high-performance devices suitable for not only previously reported in other studies electron conduction but also hole conduction. This duality opens the door to fabricating complementary logic circuits entirely from monolayer TMDs prepared via gold-assisted exfoliation.

MoS_2 n-FETs

Having established the uniformity and performance of WSe_2 p-FETs, the analysis next turns to MoS_2 n-FETs, completing the demonstration of both conduction polarities essential for CMOS applications. Transfer characteristics measured at V_{DS} = 1 V for an array of 120 MoS_2 monolayer FETs (**Figure 22a**) confirm robust n-type operation with consistent electrical behavior across the set. The reproducibility across more than one hundred devices highlights not only the reliability of the fabrication process but also the potential of gold-assisted exfoliation for generating statistically meaningful datasets, which is often a limitation in studies based solely on conventional mechanical exfoliation. A representative device measured over a range of drain biases from 0.2 V to 1 V shows the expected increase in I_{DS} under ON-state conditions, while the OFF-state current remains constant and at the level of pA/µm, demonstrating reliable electrostatic control (**Figure 22b**).

Output curves acquired for back-gate voltages between 0.5 V and 4 V exhibit a nonlinear I_{DS}–V_{DS} relation, indicative of Schottky-limited injection at the contacts (**Figure 22c**).

The distribution of threshold voltages extracted at an iso-current of 100 nA/µm (**Figure 22d**) gives a median V_{TH} of +1.2 V with a standard deviation of 0.2 V. The fact that the devices are in the off-state at zero gate bias is particularly advantageous, as it minimizes static power consumption and underlines their suitability for low-power electronics. While the spread of threshold voltage is still relatively narrow, it is broader than that observed for WSe_2 p-FETs. This difference can be partly attributed to surface residues detected by AFM (**Figure 19b**), most likely originating from PMMA used during the exfoliation process. Such contamination suggests that the gold-assisted exfoliation route may require further refinement depending on the specific 2D material employed.

The analysis of current distributions (**Figure 22e**) shows a median I_{ON} of 48 µA/µm at an overdrive of 2.4 V ($n_s = 2.3 \times 10^{13}$ cm^{-2}), with a maximum of 63 µA/µm and a standard deviation of 7 µA/µm. While these values are in line with other studies using gold-assisted exfoliated flakes[116], they remain below the performance achieved in devices fabricated from CVD- or MOCVD-grown MoS_2 monolayers, which is further discussed in the following subsection (*Comparative interpretation*). This comparison indicates that although gold-assisted exfoliation provides large-area monolayers, further improvements in both the exfoliation process and bulk crystal quality are essential. Not only the flatness and size of the parent crystal, but also its intrinsic crystalline quality, strongly influence the ultimate device characteristics. Moreover, residual PMMA contamination from the exfoliation process can increase contact resistance and

degrade carrier transport, underlining the importance of cleaner processing routes for future scalability.

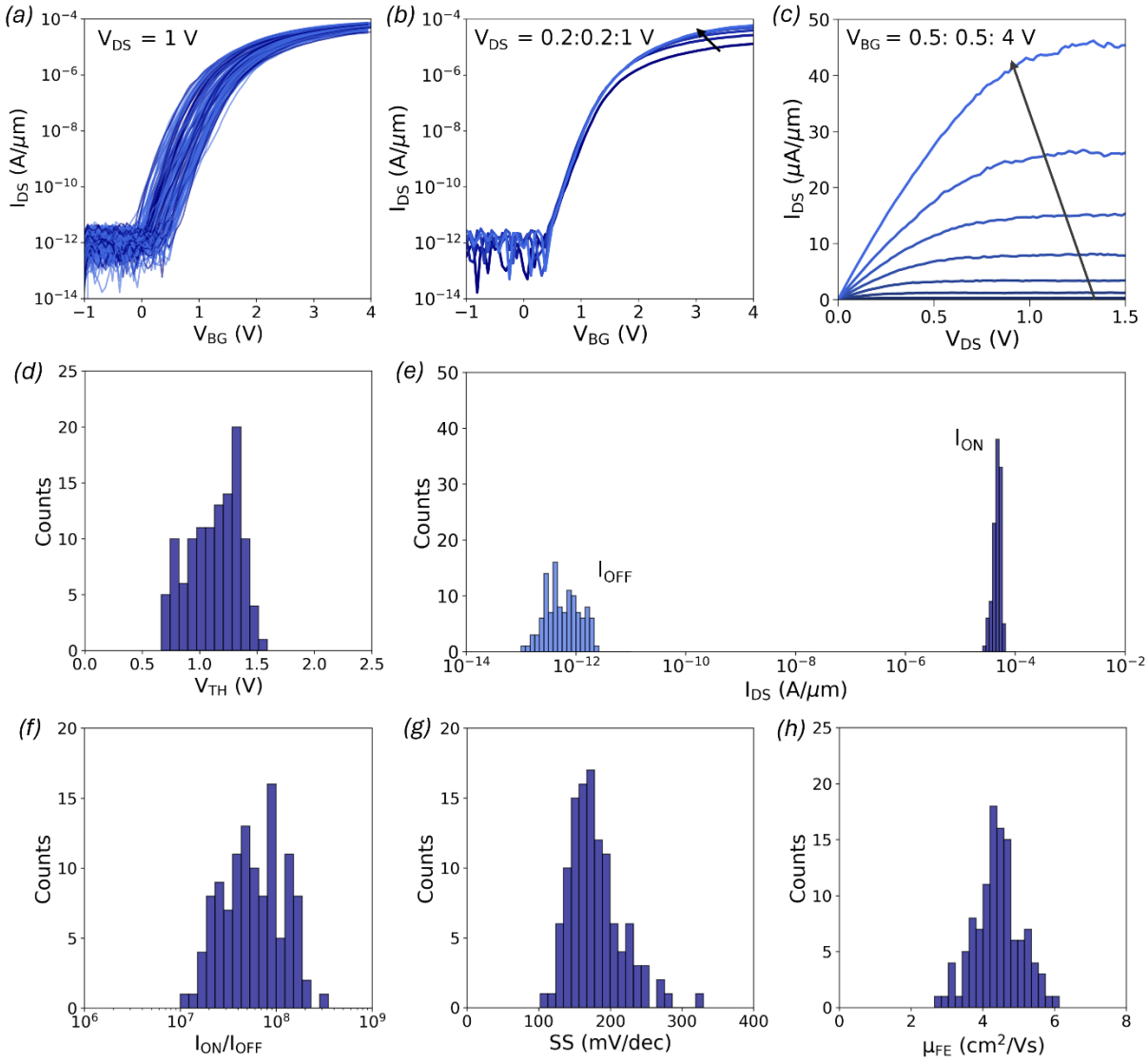

Figure 22 *Transfer curves of* ***(a)*** *120 MoS_2 n-FETs devices recorded at V_{DS} of 1V and* ***(b)*** *a representative n-FET measured at V_{DS} swept from 0.2 V to 1 V with a 0.2 V step.* ***(c)*** *Output characteristics of a representative n-FET obtained for V_{BG} varying from 0.5 V to 4 V with a step of 0.5 V. Statistical distribution of* ***(d)*** *threshold voltage (V_{TH}),* ***e)*** ON- *and* OFF-*state* currents, ***(f)*** *I_{ON}/I_{OFF} ratios,* ***(g)*** *subthreshold slopes (SS) and* ***(h)*** *field-effect mobilities (μ_{FE}).*

Despite the moderate I_{ON} levels, the distribution of I_{ON}/I_{OFF} ratios remains high, with a maximum of ~3 × 10^8 and a median of ~5.7 × 10^7 (**Figure 22f**). Such high ratios underscore efficient channel modulation and minimal leakage, key requirements for logic applications. Such values are particularly promising for ultra-low-power applications, where leakage minimization is critical. The subthreshold slope distribution (**Figure 22g**) shows a best value of 102 mV/dec and a median of 172 mV/dec, consistent with the only reported study providing

SS values for devices based on gold-assisted exfoliated MoS_2 monolayers[88]. Finally, the field-effect mobility distribution (**Figure 22f**) yields a median μ_{FE} of 4.4 cm^2/Vs (max = 6.1 cm^2/Vs). These mobilities are consistent with phonon-limited transport in short-channel MoS_2 devices with high-κ dielectrics, where remote phonon scattering from HfO_2 and interfacial charge traps dominate. The fact that the observed values approach the upper bound expected for this geometry suggests that the gold-assisted exfoliation itself does not significantly degrade channel quality. Nonetheless, the moderate SS and μ_{FE} indicate that further optimization - such as reduced polymer residues, and better contact engineering - will be required to unlock the full potential of this method for scalable, high-performance n-type devices.

Comparative interpretation

Benchmarking tables **Table 1** and **Table 2** summarize key electrical parameters for MoS_2 and WSe_2 devices fabricated using gold-assisted exfoliation, compared against devices produced via CVD, MBE, MOCVD, and conventional mechanical exfoliation.

Table 1 Benchmarking Table for WSe_2 p-FET.

Material	**Synthesis**	**Contact**	**Dielectric**	**L_{CH} (nm)**	**I_{ON} (μA/μm)**	**SS (mV /dec)**	**$\frac{I_{ON}}{I_{OFF}}$**	**Dopant**	**Ref.**
1L-WSe_2	CVT	Pd	17.5 nm ZrO_2	9400	10	60	10^6	NO_2	[117]
Multilayer -WSe_2	CVT	Pd/Pt	30 nm SiO_2	400	100	-	10^6	MoO_3	[118]
1L-WSe_2	CVD	Ti/Pd/Ni	2.8 nm HfO_2	65	300	225	10^6	NO_X	[119]
1L-WSe_2	CVD	Cr/Au	SiO_2	1800	17.9	4000	10^7	Nb	[120]
2L-WSe_2	CVT	Ti/Pt	SiO_2	-	7	~ 100	2×10^8	WO_3	[121]
1L-WSe_2	CVD	Ni/Au	120 nm SiO_2	3000	10	> 3000	10^6	Nb	[122]
1L-WSe_2	MOCVD	Pd	9nm Al_2O_3 /3nm HfO_2/ 3nm Al_2O_3	300	16	244	-	-	[123]
1L-WSe_2	CVD	Ti/Pt/Au	6 nm HfO_2	55	546	75	10^9	NO	[124]
multilayer WSe_2	MOCVD	Ru	10 nm HfO_2	140	200	7500	10^6	-	[125]
1L-WSe_2	MOCVD	Ru	4.6 nm HfO_2	50	92	180	10^8	-	[126]
2L-WSe_2	MOCVD	Pd	25 nm Al_2O_3	20	40	630	$>10^5$	WO_xSe_y layer	[127]
1L-WSe_2	MOCVD	Pd	9nm Al_2O_3 /3nm HfO_2/ 3nm Al_2O_3	300	10	450	-	-	[12]
~5L-WSe_2	Scotch tape	Pt/Pd	8 nm HfO_2	400	97	140	10^8	-	[128]
multilayer s WSe_2	Scotch tape	Pd/Au	285 nm SiO_2	3.5	20	320	10^8	-	[129]
1L-WSe_2	**gold-tape**	**Pd/Pt**	**10nm HfO_2**	**200**	**88**	**85**	**10^7**	**NO**	**This work**

In this study, the median I_{ON} values reach 48 μA/μm for MoS_2 n-FETs and 41 μA/μm for WSe_2 p-FETs, with maximum values of 63 μA/μm and 54 μA/μm, respectively. These results are in several cases comparable to, or even exceed, the I_{ON} values reported for optimized CVD- and MOCVD-grown devices. The subthreshold slopes are also competitive.

These values are consistently sharper than those reported for many devices fabricated via alternative techniques, underscoring the relatively clean interface and effective electrostatics obtained with our approach. Furthermore, the I_{ON}/I_{OFF} ratios remain high, with median values of 3×10^8 for MoS2 and 5.6×10^7 for WSe_2, placing them well within the range of best-in-class reports in the literature. On the benchmarked background of other studies, WSe_2 devices perform particularly well, demonstrating high uniformity and competitive electrical metrics, whereas MoS_2 devices, while reliable and consistent, do not stand out as exceptionally high-performing compared to the broader set of reported results.

Table 2 *Benchmarking Table for MoS_2 n-FETs.*

Material	**Synthesis**	**Contact**	**Dielectric**	**L_{CH} (nm)**	**$I_{ON}\left(\frac{\mu A}{\mu m}\right)$**	**SS (mV /dec)**	**$\frac{I_{ON}}{I_{OFF}}$**	**Ref.**
1L-MoS_2	CVD	Ni	90nm SiO_2	600	0.1	3500	10^4	51
3L-MoS_2				600	1	4000		
1L-MoS_2	MOCVD	Bi	100nm SiN_x	120	560	-	10^7	54
		Ni	300nm SiO_2	1000	2	-	10^6	
1L-MoS_2	CVD	Bi	100nm SiN_x	35	800	1670	10^6	
1L-MoS_2	CVD	Bi	300nm SiO_2	500	0.2	-	-	
1L-MoS_2	CVD	Au	30nm SiO_2	-	300	1500	$> 10^6$	46
1L-MoS_2	MBE	Au	5nm HfO_2	25	92	128	10^6	7
1L-MoS_2	MOCVD	Au	10nm HfO_2	500	120	2500	10^8	130
1L-MoS_2	CVD	Sb	100nm SiN_x	100	495	-	10^7	131
1L-MoS_2	CVD	Ni	20nm HfO_2	50	192	205	10^8	132
1L-MoS_2	gold-assisted exfoliation	Au	300nm SiO_2	1500	0.1	100	10^7	88
1L-MoS_2	CVD	Bi	100 nm SiN_x	100	544	-	10^7	131
1L-MoS_2	MOCVD	Ni	9nm Al_2O_3 /3nm HfO_2/ 3nm Al_2O_3	300	33	79	-	12
Multilayer MoS_2	scotch tape exfoliation	Ti/Au	30nm Al_2O_3	1500	1	190	10^5	133
1-15 layers MoS_2	scotch tape exfoliation	Au	90nm SiO_2	40	60	-	-	134
1L-MoS_2	**gold-assisted exfoliation**	**Au/Ti/Pt**	**10nm HfO_2**	**200**	**63**	**102**	**10^8**	**This work**

It should be noted that some of the very best CVD-grown devices still outperform current results, particularly in terms of absolute mobility and record-low SS. This performance gap can be attributed mainly to interfacial contamination introduced during the exfoliation steps and to

intrinsic defects present in the bulk crystals prior to exfoliation. Importantly, these factors are not fundamental limitations of the gold-assisted exfoliation method itself. Further refinement of the exfoliation process - particularly through improved surface cleanliness and higher-purity starting crystals - could enable performance on par with, or even surpassing, the highest-performing CVD- or MBE-grown monolayer devices.

4.4. CMOS inverter realization

Following the demonstration of reliable n- and p-type operation, the integration into complementary circuits was explored. Pairs of MoS_2 n-FETs and WSe_2 p-FETs fabricated on separate substrates were externally connected to form CMOS inverters. **Figure 23a** presents the transfer characteristics of n-FET and p-FET devices forming a representative inverter, while **Figure 23b** shows the output characteristics, demonstrating full rail-to-rail voltage swing with switching thresholds located near $V_{DD}/2$, where V_{DD} is a supply voltage.

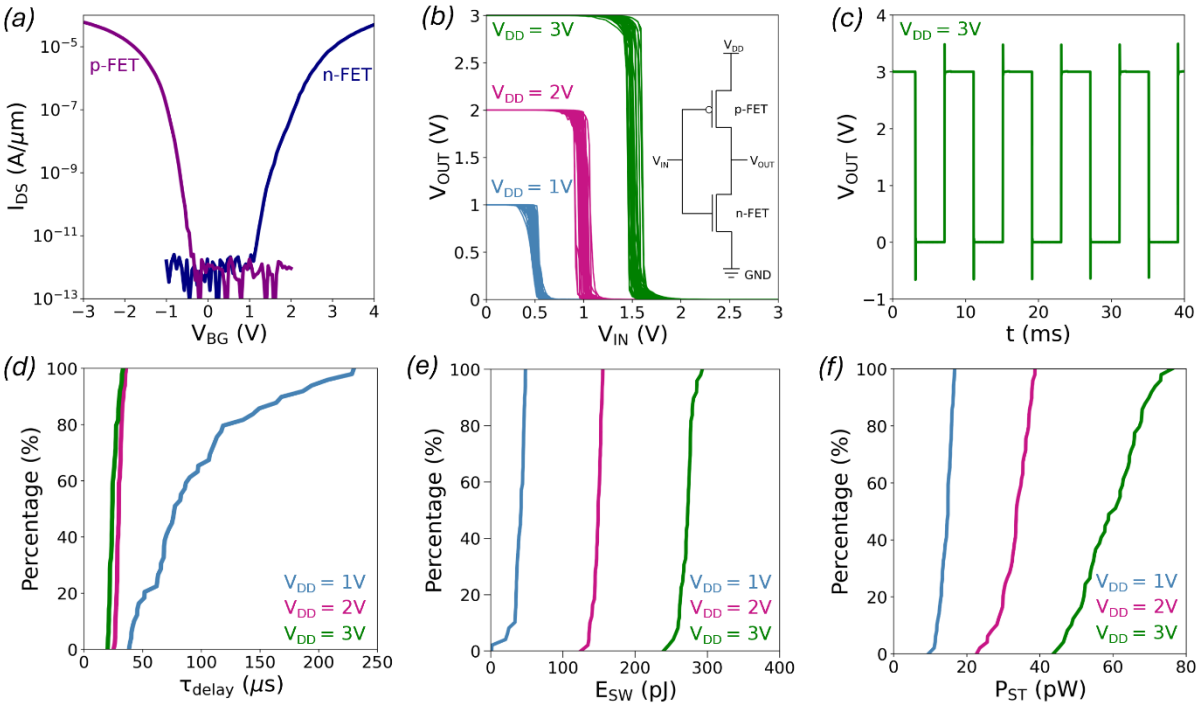

Figure 23 ***(a)*** *Transfer characteristics of representative p-FET and n-FET device recorded at a V_{DS} of 1 V.* ***(b)*** *Output curves of 50 CMOS inverters measured under supply voltages V_{DD} of 1 V, 2 V, and 3 V. Inset: schematic diagram of CMOS circuit configuration.* ***(c)*** *Output response (V_{OUT}) of a representative CMOS inverter to a square-wave input signal (V_{IN}) alternating between ground and a V_{DD} of 3 V. Cumulative distribution functions of* ***(d)*** *delay time,* ***(e)*** *static power consumption and* ***(f)*** *switching energy evaluated for V_{DD} = 1 V, 2 V and 3 V. Measurements were performed using PZ2121A high speed unit.*

This behavior arises from the symmetry in the electrical properties of the MoS_2 and WSe_2 devices, ensuring balanced switching. Although the n-FETs alone do not exhibit outstanding performance on their own, as it was show in **Figure 22**, their ON-current values are comparable to those of the p-FETs, enabling well-defined switching thresholds and robust inverter operation.

In total of 50 inverters were evaluated under supply voltages of 1, 2, and 3 V. The voltage transfer curves remain steep and symmetric across this range, while representative transient responses (**Figure 23c**) confirm clean transitions under square-wave input. Propagation delays (τ_{delay}, sum of rise and fall times) presented **Figure 23d** were extracted from the dynamic response, with the shortest values reaching 20 µs at V_{DD}=3 V (50 kHz operation). The median delay was 24 µs with a standard deviation of 4 µs, values that compare favorably with previously reported MoS_2 NMOS-only inverters[135] and nanotube-based PMOS inverters[126]. The observed decrease of τ_{delay} at higher V_{DD} , illustrates the expected trade-off between speed and power consumption.

The switching energy (E_{SW}) of a CMOS inverter quantifies the energy consumed during a single 0→1→0 (or 1→0→1) transition of the output node. It can be expressed as **Equation 23**:

$$E_{SW} = V_{DD} \int |I(t)| dt \qquad \textbf{Equation 23}$$

where I(t) is the transient current drawn from the power supply during charging and discharging of the output node. Physically, this integral represents the total charge moved through the device in a switching event, and its product with V_{DD} corresponds to the energy dissipated (mainly as Joule heating) when charging/discharging the load and parasitic capacitances, with an additional contribution from short-circuit current flowing when both transistors conduct simultaneously. **Figure 23e** presents the distribution of E_{SW}, which at V_{DD}=3 V showed a median of ~273 pJ, a minimum of 239 pJ, and a standard deviation of 10 pJ.

In addition to dynamic dissipation, static power consumption (P_{ST}) is determined by leakage currents that flow when the inverter is in a steady state. It is given by **Equation 24**:

$$P_{ST} = V_{DD} I_{ST} \qquad \textbf{Equation 24}$$

where I_{ST} is the leakage current of the inverter in its logic '0' or '1' state. Thanks to the extremely low leakage currents of the MoS_2 and WSe_2 FETs (**Figure 24a,b**), I_{ST} remains in the pA/µm range, leading to sub-100 pW dissipation even at V_{DD}=3 V (**Figure 23f**). More precisely, P_{ST} values ranged from 44 to 78 pW with a median of 60 pW, substantially below

typical values for other nanomaterial-based inverters[135–137]. The rise of both P_{ST} and E_{SW} with supply voltage reflects the fundamental balance between energy efficiency and faster switching.

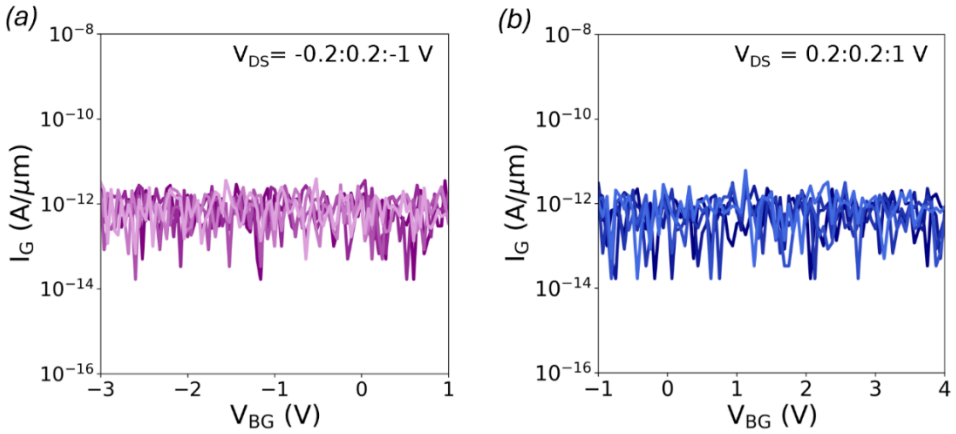

Figure 24 *Gate leakage current (I_G) of* ***(a)*** *p-FET and* ***(b)*** *n-FET devices acquired across different V_{DS} values. In both device types, I_G stays at the pA/μm level and shows no dependance on either of V_{DS} and V_{BG}.*

When benchmarked against prior demonstrations of 2D CMOS, the presented inverters combine low propagation delay, minimal static dissipation, and symmetric transfer curves that collectively surpass many reported results[126,135–137]. These advances stem directly from the matched MoS_2 and WSe_2 devices obtained via gold-assisted exfoliation. Although the present circuits were assembled by external wiring, future monolithic integration on a single substrate is expected to further improve speed, noise margins, and scalability, reinforcing the potential of this method for energy-efficient 2D logic.

4.5. Assessment of Applicability

Given that gold-assisted exfoliation relies on monolayers obtained directly from bulk single crystals, one might expect device performance to surpass that achieved with CVD- or MOCVD-grown materials. However, the results presented here show that the electrical characteristics of devices fabricated using this approach remain at a comparable level. Consequently, there are no clear indications that this method should be prioritized for optimization toward industrial implementation of 2D FETs, especially considering that such adaptation would be technically demanding. While the method enables the preparation of large-area, high-quality monolayers with uniform structural and electronic properties, its practical implementation outside the laboratory is far from straightforward. The process involves delicate handling, reliance on gold tape, and susceptibility to contamination, all of which complicate reproducibility under the strict standards of industrial semiconductor fabrication. Scaling the process to wafer-level

production would require substantial modifications and careful engineering of equipment, making the transition to mass manufacturing both costly and resource-intensive.

The real strength of gold-assisted exfoliation lies in its role as a research and prototyping tool. Beyond FETs and CMOS inverters, high-quality monolayers obtained this way can be broadly useful in areas like optoelectronics and photodetection[31], chemical and biosensing[138], and (photo-/electro-)catalysis[139]. In these contexts, reproducible access to clean, uniform monolayers enables rapid exploration of device physics and materials phenomena, making gold-assisted exfoliation especially valuable in academic and early-stage technology studies.

Presented work showed that gold-assisted exfoliation provides a reliable platform for producing statistically significant arrays of both n- and p-type FETs, enabling systematic device studies that are difficult to achieve with conventional exfoliation. The resulting devices exhibit competitive ON-currents, sharp subthreshold slopes, high ON/OFF ratios, and reproducible threshold voltages. Furthermore, CMOS inverters constructed from these gold-exfoliated n- and p-FETs demonstrate reliable complementary logic operation with sharp voltage transfer characteristics, symmetric switching thresholds, fast transient response, and low static power consumption. However, when compared to state-of-the-art silicon CMOS inverters, the devices realized here cannot yet compete in absolute performance metrics such as ON-current or subthreshold slopes, where silicon technology still leads[140]. Therefore, the true applicability of gold-assisted exfoliation is best seen in exploratory studies, including the development of heterostructures aimed at reducing contact resistance or fabricating high-performance top-gate dielectric stacks. The demonstration of the applicability of gold-assisted exfoliation for such heterostructures will be discussed in detail in the following chapters.

Chapter 5. Contact resistance engineering in TMD-based FETs using vdW interlayer

This chapter is based on the publication: Giza et al., 'Contact Resistance Engineering in WS_2-Based FET with MoS_2 Under-Contact Interlayer: A Statistical Approach', *ACS Applied Materials & Interfaces* 2024, 16 (36), 48556–48564. DOI: 10.1021/acsami.4c09688, in which I am the first author.

5.1. Role of Fermi level pinning at metal/semiconductor interfaces

Charge injection in 2D semiconductor FETs is strongly influenced by FLP at the metal - semiconductor junction. In an ideal Schottky contact, the barrier height is determined by the difference between the metal work function and the semiconductor electron affinity (Schottky-Mott rule). However, in practice MIGS and other interface defects pin the semiconductor Fermi level, making the Schottky barrier nearly independent of the metal's work function. In ultrathin TMDs, damage introduced during fabrication (e.g. from resistive or electron beam evaporation[141,142]) gives rise to a high density of interface states, which strongly enforces FLP. As a result, changing the metal usually has little effect on barrier height. This unfavorable FLP leads to large, unpredictable Schottky barriers and high contact resistance in 2D FETs.

Among the main factors responsible for Fermi-level pinning in TMDs are MIGS. MIGS are metal states that extend into the TMD bandgap. MIGS can accumulate a large amount of charge, which causes the semiconductor level to align with surface states (gap states) more preferably than with the metal Fermi level, pinning the Fermi level. Reducing MIGS is therefore key to mitigating FLP. For example, using semimetals with vanishing density of states (such as Bi[54]) at the Fermi level suppresses MIGS and yields very low contact resistance on WS_2 and MoS_2. Other strategies include chemical or molecular doping[143,144] to shift the TMD Fermi level and insertion of buffer layers. Inserting a 2D dielectric[145,146] or 2D semiconducting[147] buffer layer decouples the metal from the TMD and can dramatically lower the contact resistance.

In the reported results, however, the effectiveness of these approaches is usually demonstrated on only a handful of devices, often highlighting the best-performing examples. Such limited datasets can be misleading, as they may mask the variability that naturally arises from sample-to-sample differences, local inhomogeneities, or processing-induced contamination common in 2D systems. Without sufficient statistics, it is difficult to distinguish whether a reported improvement reflects a genuine, robust trend or simply an outlier. In many cases, these limitations stem from the use of mechanically exfoliated flakes, which inherently restrict the

number of devices that can be fabricated and measured, thereby biasing the analysis toward limited device counts.

Comprehensive studies that systematically apply these strategies across large arrays of devices are still missing. Statistical evaluation is crucial for identifying the true distribution of key parameters such as contact resistance, threshold voltage, or mobility, and for quantifying device-to-device reproducibility. Only such analyses can reveal whether a given contact engineering method is broadly effective, scalable, and compatible with integration, or whether its success is limited to isolated cases. The absence of these studies leaves significant uncertainty about the reliability of even the most promising strategies, and represents a critical gap in the current literature.

5.2. Au/MoS_2/WS_2 contact structure design

In this work, an alternative FLP-suppression strategy is evaluated on a statistically significant number of devices, overcoming the limited scope of previous reports. Specifically, an Au/MoS_2/WS_2 contact geometry was designed and implemented, where the Au electrode is deposited on top of a monolayer MoS_2 serving as the under contact interlayer (UCI), while the channel consists of pristine WS_2. The incorporation of the UCI is intended to mitigate FLP. In this configuration, FLP occurs at the Au/MoS_2 interface rather than directly at the Au/WS_2 junction, which is important because the level of pinning in metal/2D-TMD systems is known to be almost independent of the metal work function[14], but strongly dependent on the particular TMD used[36]. This dependence arises because the Fermi level is pinned near the charge neutrality level (CNL), which varies among different semiconductors as a consequence of their distinct interfacial density of states and electronic structure. Importantly, the effective work function of the Au/MoS_2 system is lower than that of Au in direct contact with WS_2, as demonstrated in both theoretical and experimental studies[34,148]. Since the pinning energy level (E_{FP}) differs for Au/MoS_2 and Au/WS_2 junctions, the Schottky barrier height (ϕ_{SB}) is given by the relation **Equation 25**[147]:

$$\Phi_{SB} = E_{FP} - X \qquad \textbf{Equation 25}$$

Thus, inserting MoS_2 underneath the Au modifies the effective pinning level, shifting it closer to the conduction band and yielding, in principal, a smaller barrier compared to direct Au/WS_2.

The mechanism behind this improvement is twofold. First, the effect of pinning is strongest only in the first layer directly touching the metal[149], so the introduction of MoS_2 as an interlayer effectively screens the underlying WS_2 from direct FLP. This is particularly advantageous, as

it enables band-engineering without altering the pristine nature of the WS_2 channel itself. Second, the conduction-band alignment at the MoS_2/WS_2 interface further facilitates charge injection: the conduction band minimum of MoS_2 has lower affinity than that of WS_2[24], so electrons entering from the metal encounter a favorable step into the WS_2 channel. This cascade-like energy alignment effectively funnels carriers into the conduction band of WS_2, lowering the overall injection barrier.

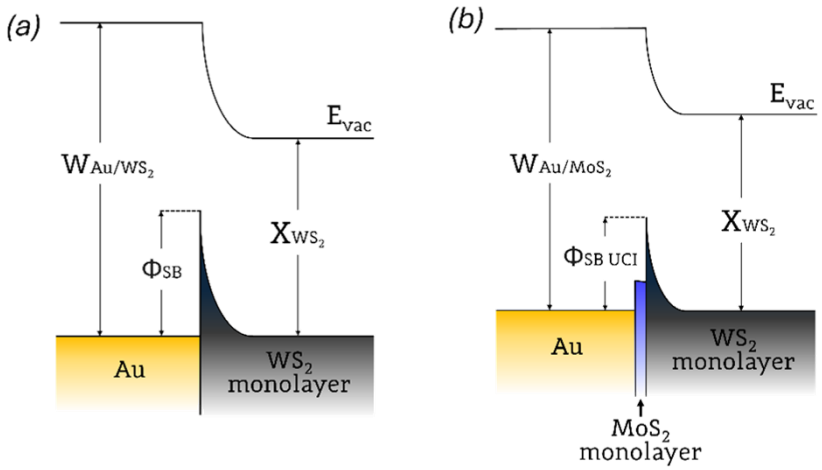

Figure 25 *Schematic illustration of band alignment for* ***(a)*** *Au/WS2 junction and* ***(b)*** *Au/MoS_2/WS_2 junctions. W – work function, X – electron affinity, Φ_{SB} – Schottky barrier height.*

As a result, the Au/MoS_2/WS_2 stack is expected to exhibit a significantly reduced Schottky barrier height ($\Phi_{SB\ UCI}$) relative to the conventional Au/WS_2 contact, yielding improved electron injection and lower contact resistance. This effect is clearly illustrated in energy-band diagrams presented in **Figure 25**, where the barrier at the Au/MoS_2/WS_2 junction is not only smaller, but also exhibit step-like alignment. Consistent with these predictions, this engineered geometry was expected to cause the reduction in contact resistance compared to direct Au/WS_2 contacts.

5.3. Fabrication of WSe_2 FETs with MoS_2 under-contact interlayer

To realize this unique contact geometry, a dedicated fabrication method for assembling van der Waals heterostructures was developed specifically for this work, which constitutes a major advantage of the present study. The approach combines precise patterning of monolayers by lithography and reactive ion etching with their subsequent transfer mediated by gold, allowing placement of nanoscale features onto another 2D material.

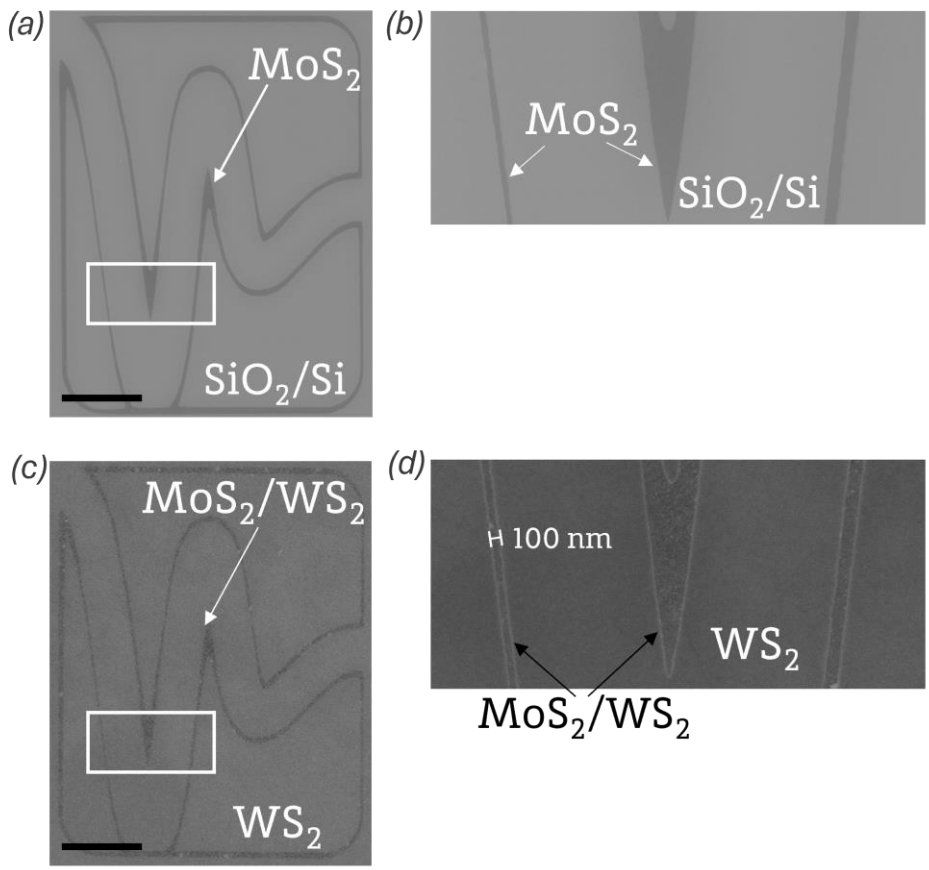

Figure 26 (a) *SEM image of a patterned and etched MoS_2 monolayer on a SiO_2/Si substrate forming the Faculty of Physics WUT logo (scale bar: 4 µm).* ***(b)*** *Magnified view of the region marked by the white rectangle in panel* ***(a)****.* ***(c)*** *SEM image of the transferred logo using the gold-assisted method onto a WS_2 monolayer, resulting in a MoS_2/WS_2 van der Waals heterostructure (scale bar: 4 µm).* ***(d)*** *Magnified view of the area highlighted by the white rectangle in panel* ***(c)****.*

Before applying this method to device fabrication, its capabilities were demonstrated using a model structure patterned in the shape of the Faculty of Physics WUT logo. Scanning electron microscope (SEM) images (**Figure 26a,b**) show a patterned and etched MoS_2 monolayer on a SiO_2/Si substrate, while further images (**Figure 26c,d**) confirm that a patterned MoS_2 monolayer can be reliably transferred onto a WS_2 monolayer to form a MoS_2/WS_2 heterostructure. Importantly, even features as narrow as 100 nm retained their shape and continuity after transfer, highlighting the high fidelity of the process. All SEM images were acquired with an InLens secondary electron detector in the Raith e-Line Plus system. Complementary AFM imaging and Raman mapping further validated the successful assembly of the heterostructure (**Figure 27**). The Raman maps reveal the characteristic MoS2 E_{2g} (~382 cm^{-1}), WS_2 A_{1g} (~417 cm^{-1}), and Si (~521 cm^{-1}) modes, with reduced Si intensity in the heterostructure area due to stronger light absorption. The MoS_2 and WS_2 intensity distributions

confirm the presence of both monolayers, while the enhanced WS_2 A_{1g} mode in the overlapping region reflects interlayer interactions. In this study, a laser with a wavelength of 532 nm was used, and the laser power was kept below 0.5 mW to avoid damaging the material. AFM scans (Figure 27d,e) show uniform topography and thickness consistent with the value expected for monolayer (0.8 nm), further supporting the successful transfer.

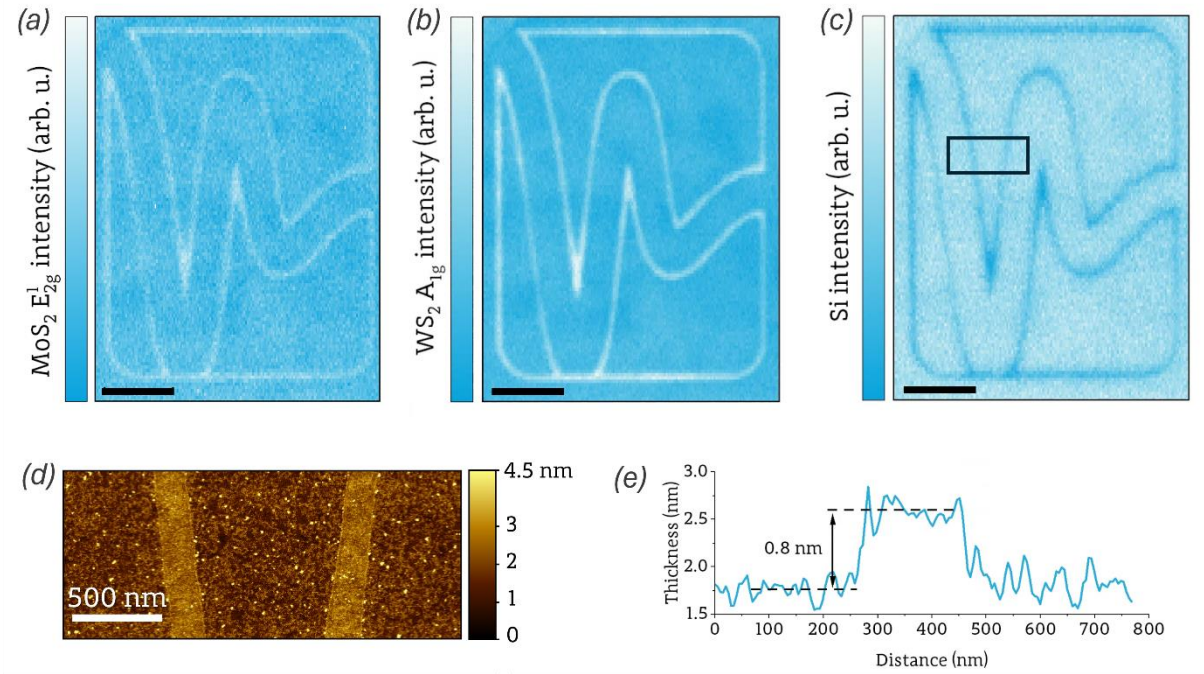

Figure 27 *Raman mapping and AFM characterization of MoS_2/WS_2 heterostructure patterned as the Faculty of Physics WUT logo. Raman maps show intensity signals of* ***(a)*** *MoS_2 E_{2g} mode (382 cm^{-1}),* ***(b)*** *WS_2 A_{1g} mode (417 cm^{-1}) and* ***(c)*** *silicon peak (521 cm^{-1}). Scale bars correspond to 4 µm. (d) AFM height image of heterostructure region highlighted by a black rectangle in* ***(c)****.* ***(e)*** *Height profile measured across one of the transferred stripes in* ***(d)****. Measurements were performed using Bruker Dimension Icon AFM and Renishaw inVia Qontor Raman spectrometer.*

Having established the feasibility of transferring pre-patterned monolayers while preserving nanoscale resolution, the method was next applied to the fabrication of MoS_2/WS_2 heterostructures for device integration. To clarify how this approach operates, the fabrication process is described in detail below, which relies on the gold-assisted transfer of pre-patterned MoS_2 monolayers (**Figure 28**). First, large-area monolayer MoS_2 is obtained by gold-assisted exfoliation onto SiO_2/Si and identified by optical microscopy. This continuous MoS_2 film is then patterned by electron beam lithography followed by O_2 RIE etching into narrow stripes defining the future contact regions. The use of dry etching at this stage ensures atomically sharp edges of the interlayer, which is critical for ensuring reproducible device geometry.

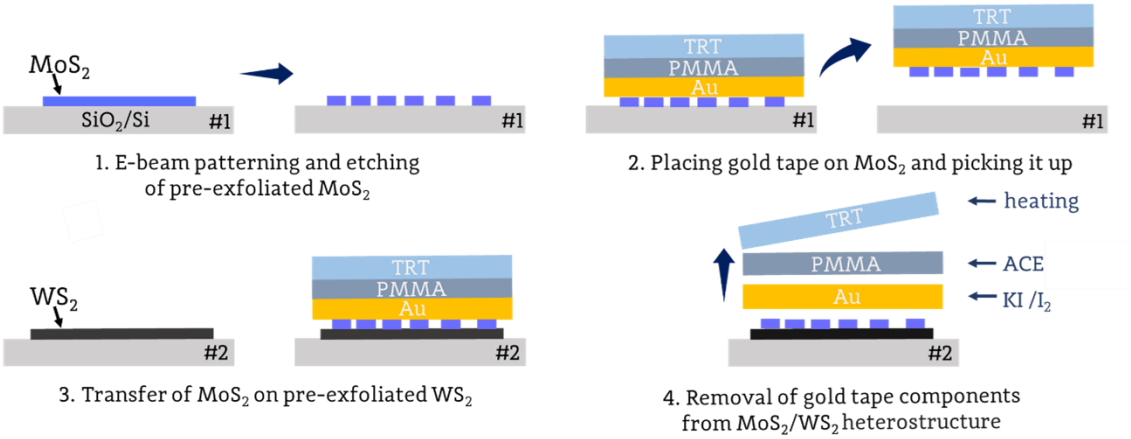

Figure 28 *Schematic illustration of the gold-assisted transfer procedure. The symbol "#number" denotes individual SiO_2/Si substrates.*

After that, gold tape is placed on the sample, covered with a glass slide, and loaded with a weight of approximately 120 g for 20 minutes to promote strong adhesion between the Au layer and the patterned MoS_2. To further strengthen the interface, the stack is annealed on a hot plate at 150 °C for 20 minutes. At elevated temperature, TRT detaches, leaving the MoS_2/Au/PMMA stack firmly attached to the substrate. After cooling, a fresh TRT is applied and the MoS_2/Au/PMMA/TRT stack is peeled off with tweezers. The obtained stack is then aligned and brought into contact with a separate substrate containing a monolayer WS_2 prepared by gold-assisted exfoliation on SiO_2/Si (285 nm of SiO_2). As in the previous step, the sample is covered with a glass slide, pressed with a 120 g weight for 20 minutes to ensure strong adhesion, and annealed again at 150 °C for 20 minutes. During annealing, the TRT detaches, and subsequent removal of the gold and PMMA layers (same procedure as described in 4.2) leaves the pre-patterned MoS_2 stripes positioned on top of the WS_2 film. Importantly, the approach enables parallel transfer of many features in a single step: optical microscopy revealed heterostructure arrays covering areas exceeding 0.5×10^6 μm^2 in one transfer process (**Figure 29a**). Such scalability is difficult to achieve with conventional deterministic pick-and-place methods (e. g., PDMS-, PC-assisted methods), highlighting the robustness of the gold-assisted transfer technique.

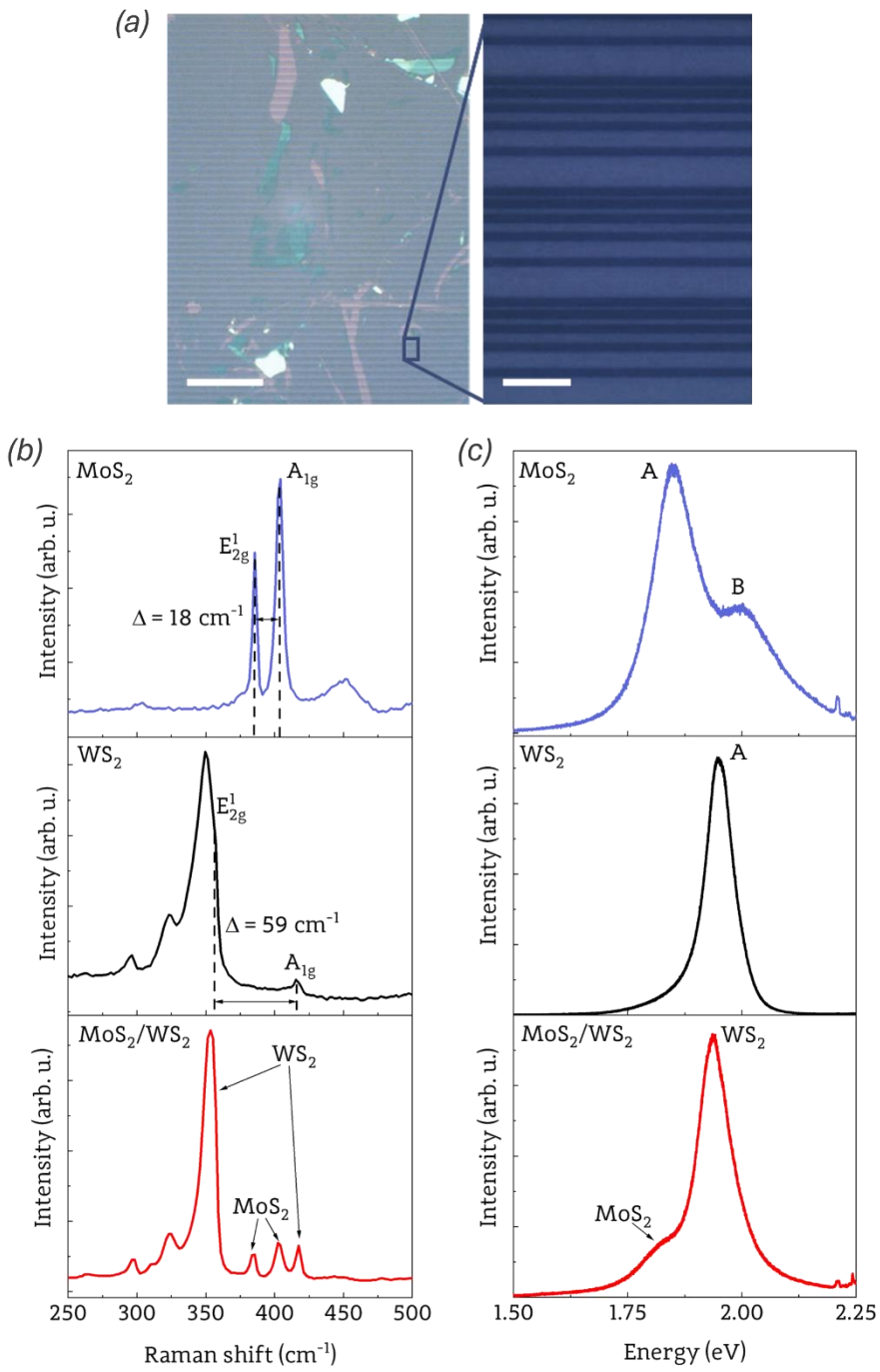

Figure 29 (a) *Example of a heterostructure consisting of MoS_2 monolayer stripes transferred onto a continuous WS_2 monolayer. Scale bars: 150 µm (left) and 10 µm (right).* ***(b)*** *Raman spectra and* ***(c)*** *PL spectra of MoS_2, WS_2, and the MoS_2/WS_2 heterostructure.*

Confirmation of MoS_2/WS_2 heterostructure formation was further supported by Raman and photoluminescence spectroscopy (**Figure 29b,c**), which revealed the characteristic peaks of both materials, thereby validating the successful assembly of the heterostructure . The Raman spectra of MoS_2, WS_2, and the MoS_2/WS_2 heterostructure show the expected E_{2g} and A_{1g} modes (**Figure 29b**), with their positions determined by Lorentzian fitting. The peak separations of

18 cm^{-1} for MoS_2 and 59 cm^{-1} for WS_2 confirm the monolayer character of both materials[150,151]. In the heterostructure spectrum, the contributions from each component layer are clearly visible and are marked with arrows. Photoluminescence measurements (**Figure 29c**) further support this: the MoS_2 monolayer exhibits both A and B exciton peaks, while the WS_2 spectrum displays only the A exciton peak, consistent with monolayer behavior[152,153]. In the MoS_2/WS_2 heterostructure spectrum, the characteristic excitonic features of the individual monolayers are preserved and highlighted, confirming successful stacking without significant degradation of their optical properties. Taken together, these results demonstrate that gold-assisted stamping of patterned monolayers offers a scalable route to assemble complex van der Waals heterostructures with controlled geometry, well-suited for integration into complex device architectures.

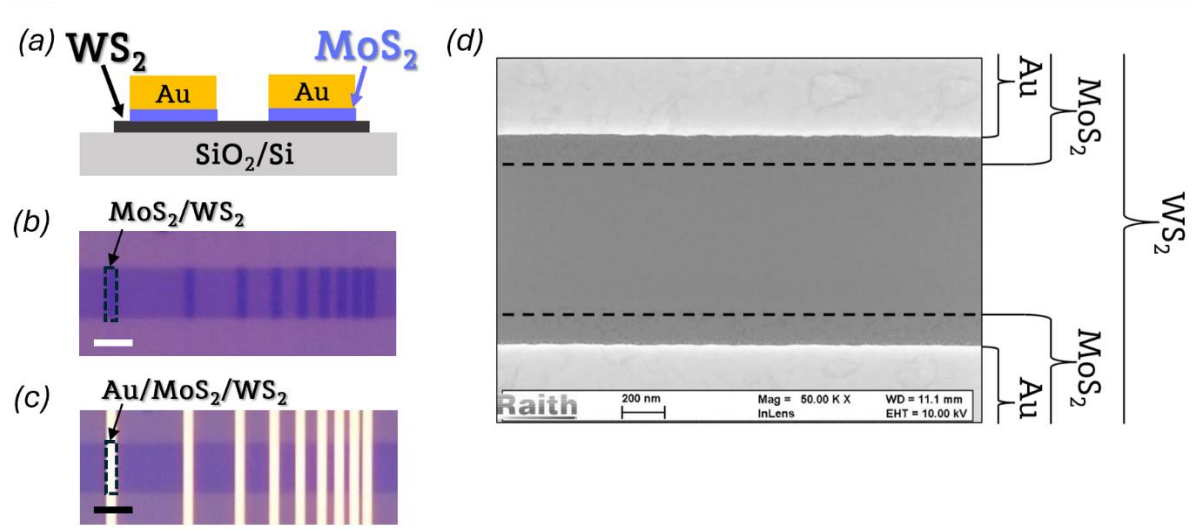

Figure 30 (a) *Schematic illustration of the device with UCI.* ***(b)*** *Optical image of the heterostructure MoS_2 stripes with varying spacing on a WS_2 layer.* ***(c)*** *Optical image of the fabricated device with gold contacts evaporated on the heterostructure area, creating a configuration that enables the use of the TLM method.* ***(d)*** *SEM image of the representative device with UCI, which proves that MoS_2 extends beyond gold contacts.*

To fabricate FETs (**Figure 30a**) from the obtained MoS_2/WS_2 heterostructures, the device channel width was first defined by electron beam lithography and RIE etching (**Figure 30b**). Subsequently, source and drain contacts were patterned by electron-beam lithography, followed by thermal evaporation of a 70 nm Au layer, yielding well-defined $Au/MoS_2/WS_2$ junctions (**Figure 30c**). In devices incorporating the ultrathin contact interlayer, MoS_2 stripes were patterned to a length of 1.3 µm, while the Au contacts were designed with a length of 1 µm to avoid any direct overlap with the underlying WS_2 layer (**Figure 30d**). The transferred MoS_2 stripes defined the channel lengths, which ranged from 0.5 to 8 µm, while the channel width

was fixed at 6 µm for all structures. Notably, the contact stripes were positioned with varying spacing, which was crucial for applying the TLM to determine contact resistance. To provide a direct comparison, a series of reference devices based solely on monolayer WS_2 (without MoS_2) were also realized, maintaining identical channel dimensions and contact geometry.

5.4. Statistical evaluation of interlayer effect on FET performance

Having established a consistent fabrication protocol for both reference WS_2 devices and heterostructure-based transistors with a MoS_2 under-contact interlayer, the next step was their electrical characterization. Measurements were carried out in high vacuum (~10^{-6} mbar) at room temperature inside a cryostat. Prior to testing, the samples were kept under vacuum for 19 h, including a 13 h annealing step at 200 °C, in order to remove adsorbates and improve contact stability. Since the cryostat setup required the devices to be physically connected to the measurement adapter, wire bonding with aluminum wires was used to link the Au pads on the chips to the adapter.

Under these well-controlled conditions, a large statistical study was performed on 160 FETs (80 with MoS_2 under the contacts, 80 without) with identical channel and contact geometries. This allowed reliable extraction of R_c and other figures of merit.

The measurements were carried out in a back-gated configuration, where 285 nm of SiO_2 served as gate dielectric. All electrical measurement was performed using DL Instruments 1211 Current Preamplifier, National Instruments DAQ 6366, and source measuring unit Keithley 2450. Representative transfer curves for devices with and without the UCI (**Figure 31a**) clearly demonstrate that the insertion of the MoS_2 layer leads to a reduction in threshold voltage and a significant increase in the on-state current. Similarly, the output characteristics (**Figure 31b,c**) show that the source-drain current in devices with UCI is approximately three times higher than in bare WS_2 FETs. The qualitative shape of the output curves remains nonlinear in both cases, revealing Schottky-type transport at both types of contacts.

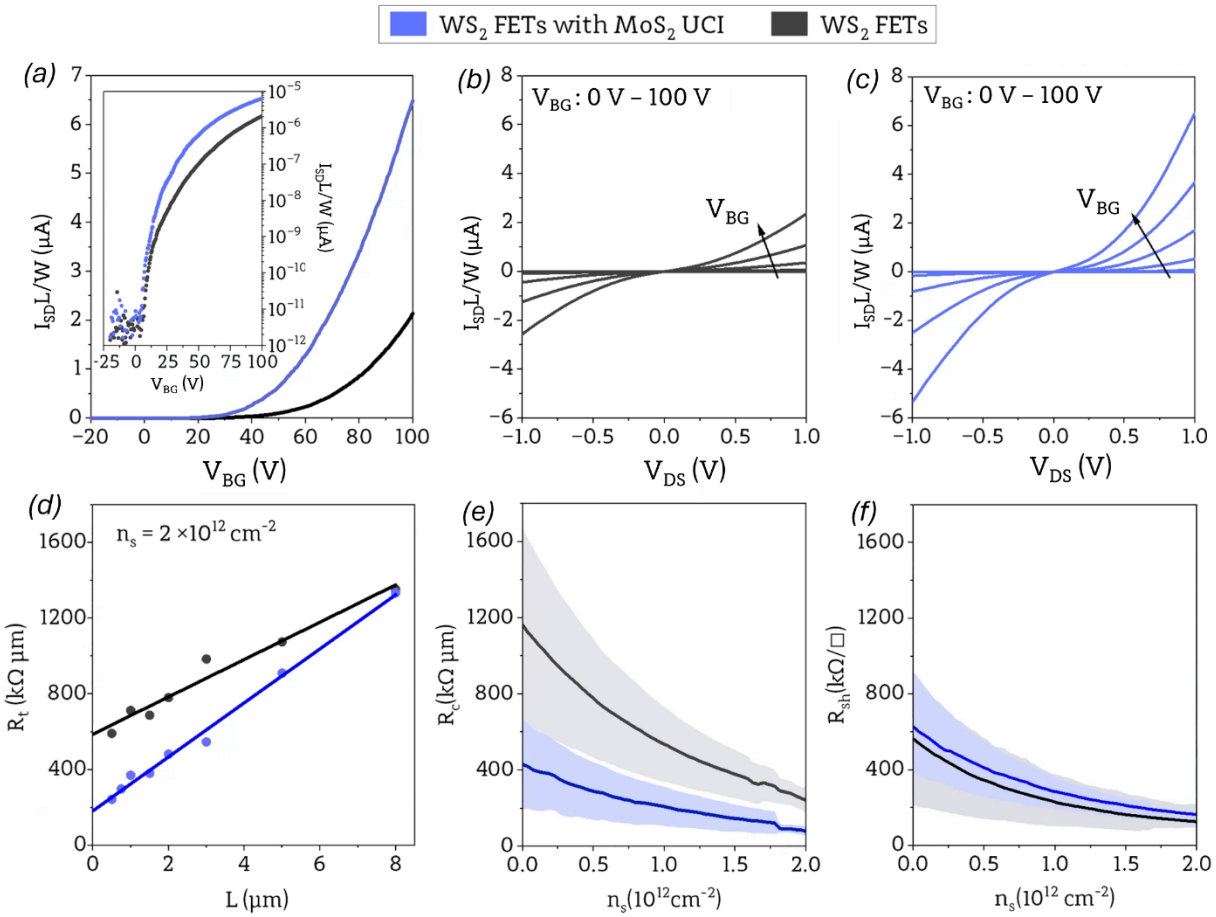

Figure 31 ***(a)*** *Transfer characteristics on linear scale for representative devices with and without UCI. Inset: corresponding semilogarithmic plot. All measurements were performed with V_{DS} = 1 V.* ***(b)*** *Output characteristics of a representative device without UCI, recorded for gate voltages from 0 V to 100 V, with a 20 V step, and* ***(c)*** *for a representative device with a UCI.* ***(d)*** *Dependence of total contact resistance (R_t) on channel length (L), calculated at a carrier concentration of n_s=2×10^{12} cm^{-2} for two representative TLM sets with fitted linear function for R_c extraction.* ***(e)*** *Mean value and standard deviation of contact resistance (R_c) as a function of carrier concentrations.* ***(f)*** *Mean value and standard deviation of sheet resistance (R_{sh}) versus carrier concentrations.*

Figure 31d shows the representative results of R_t-L at the overdrive voltage corresponding to the carrier concentration of n_s=2×10^{12} cm^{-2}, as determined from **Equation 1**, along with a linear fit used to determine R_c and R_{sh} according to **Equation 21**. The same analysis was carried out for other n_s values for 13 TLM structures with and without UCI. The resulting mean values and standard deviations of R_c and R_{sh} for devices with and without UCI are summarized in **Figure 31e,f**. The values of R_c and R_{sh} are highly sensitive to the n_s. The gate voltage not only tunes the carrier concentration in the transistor channel but also influences the channel–contact interface. This phenomenon, referred to as contact gating, is characteristic of devices with a global back-gate architecture. In such a configuration, the applied back-gate voltage narrows the Schottky barrier at the contact, thereby facilitating carrier tunneling across the junction and

consequently lowering R_c. The presence of the MoS_2 interlayer reduced R_c by over 60%. For example, at a carrier concentration of 2×10^{12} cm^{-2}, devices without the interlayer had a mean $R_c = 242$ kΩ·μm ($\sigma = 72$ kΩ·μm), whereas devices with the MoS_2 interlayer had $R_c = 79$ kΩ·μm ($\sigma = 27$ kΩ·μm). This large drop confirms the favorable band alignment for $Au/MoS_2/WS_2$. The reduced variance in R_c for the UCI devices ($\sigma = 27$ vs 72) also indicates more uniform contacts. At the same time, no significant change in R_{sh} is observed, with the difference falling within the standard deviation. This indicates that the channel material remains essentially unaffected during the transfer process, and that the MoS_2 interlayer influences only the contact region.

To capture device-to-device variability in a statistically meaningful way and to evaluate how reduced contact resistance influences 2D-FET performance, **Figure 32** summarizes the key parameters: V_{TH}, μ_{FE}, SS, and I_{ON}/I_{OFF} for devices with different channel lengths (L). FETs with the interlayer consistently had lower threshold voltages (from 45 to 70 V). Without MoS_2, V_{TH} clustered around ~70 V for all channel lengths (**Figure 32a**). The reduction in V_{TH} observed in UCI devices can be attributed to the lower Schottky barrier height at the $Au/MoS_2/WS_2$ contact. In bare WS_2 devices, the higher barrier requires a larger positive gate voltage to induce sufficient carrier injection, whereas the presence of the MoS_2 interlayer lowers the barrier, enabling channel turn-on at smaller gate biases. With MoS_2, V_{TH} values were not only lower but also showed some channel-length dependence (shifting negatively as length decreased). The observed increase of V_{TH} for shorter channels is consistent with the contact-limited nature of the devices: as the relative contribution of the contact resistance to total resistance becomes more significant at smaller L, a larger gate bias is required to induce sufficient carrier injection through the Schottky barrier, effectively shifting V_{TH} to higher values.

Figure 32b represents the distribution of μ_{FE}. Calculated values were higher in devices with the interlayer. Although both sets of devices had identical WS_2 channel areas, the UCI devices showed systematically larger μ_{FE} for every channel length. This is understood as a contact-limited effect: μ_{FE} in short-channel devices is degraded by contact resistance, so lowering R_c by use of the interlayer raises the measured mobility. In practice, μ_{FE} reached close to 20 cm^2/Vs in both cases, but the UCI devices attained higher values at different channel lengths.

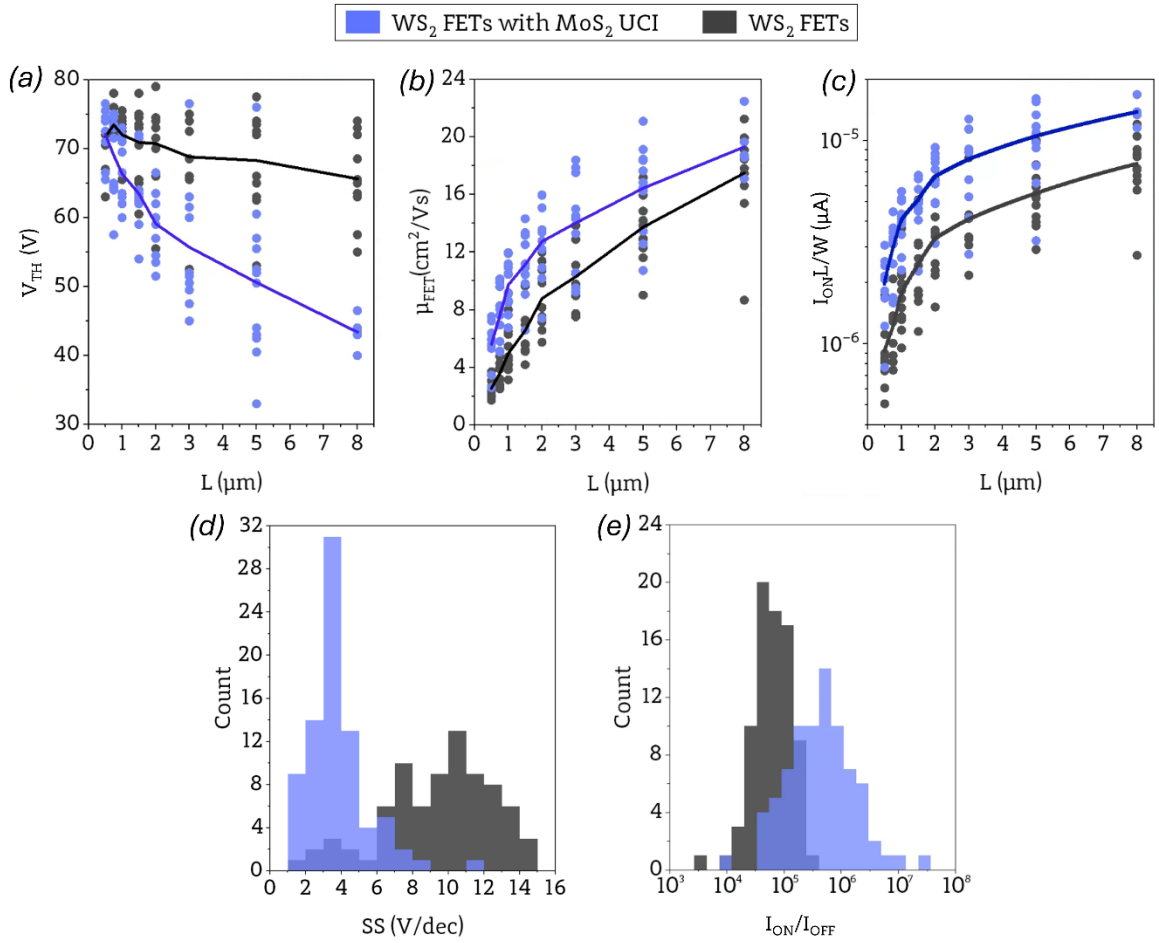

Figure 32 *Distribution of* ***(a)*** *threshold voltage,* ***(b)*** *field-effect mobility, and* ***(c)*** *ON-state current (I_{ON}) for devices with and without UCI across different channel lengths; solid lines indicate mean values.* ***(d)*** *Histograms of subthreshold swing (SS) and* ***(e)*** *I_{ON}/I_{OFF} ratios for devices with and without UCI.*

Moreover, FETs with UCI carried higher ON-currents (**Figure 32c**). Again, strong dependence on L is observed, which is consistent with the previous observation of the influence of R_c on μ_{FE}. **Figure 32d** presents the distribution of SS. Both device types exhibit relatively high SS values due to the use of a 285 nm-thick gate oxide. For devices without the UCI, the SS distribution peaks at approximately 11 V/dec, while devices incorporating the MoS_2 interlayer show a peak around 3 V/dec, more than three times lower. The subthreshold swing is evaluated over gate voltages below the threshold and reflects how sharply the device transitions from the off-state to the on-state.

Consequently, devices with a higher Schottky barrier and increased contact resistance display larger SS values, indicating a slower channel turn-on and reduced charge injection efficiency. This improvement in switching sharpness is further evidenced by the I_{ON}/I_{OFF} ratio (**Figure 32e**), which increases by roughly an order of magnitude: the mode of the I_{ON}/I_{OFF} distribution

reaches ~10^6 for UCI devices compared to ~10^5 for devices without the interlayer. Such a tenfold enhancement underscores how mitigating the contact resistance bottleneck strengthens the transistor performance.

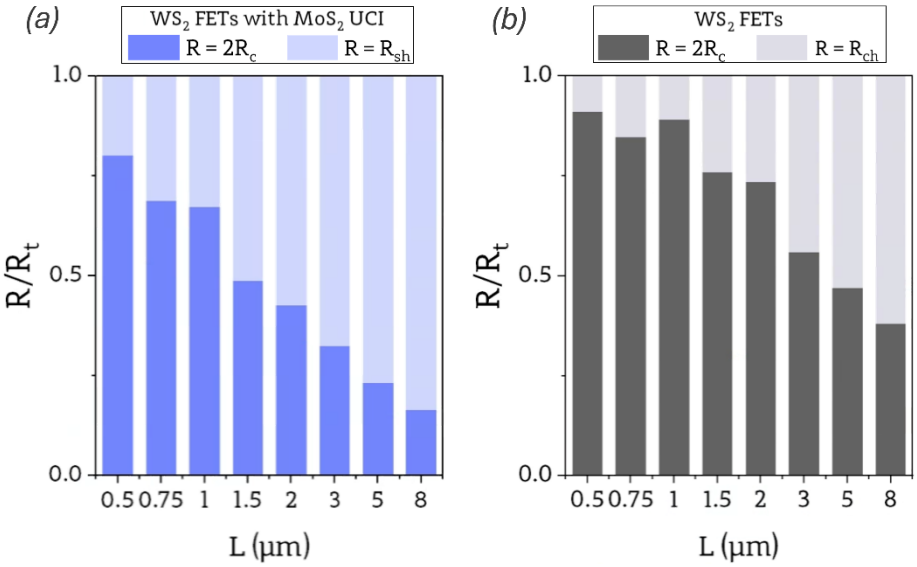

Figure 33 *Stacked bar plots of R_{ch} and R_c contribution to the total resistance R_t of devices* ***(a)*** *with UCI and* ***(b)*** *without UCI.*

To further study the impact of contact resistance on device behavior at different channel lengths, **Figure 33a,b** presents stacked bar plots of the channel resistance (R_{sh}) and total contact resistance ($2R_c$) contributions to the mean total resistance (R_t) for representative channel lengths, for devices with UCI and without UCI. The fraction of the total resistance attributed to contacts ($2R_c/R_t$) is much larger for shorter channels and diminishes as the channel length increases. However, this trend differs between the two device types. In the interlayer devices (**Figure 33a**), the proportion of contact resistance drops steeply with increasing L, indicating that at longer channel lengths the device resistance is dominated by the channel itself. By contrast, in devices without the interlayer (**Figure 33b**), even at the longest channel lengths measured, roughly over one third of the total device resistance still originates from the Au/WS_2 contacts. The result is in good agreement with the channel-length dependence of V_{TH} and μ_{FE} observed in **Figure 32a,b**, further highlighting how contact resistance shapes the electrical characteristics of the devices.

5.5. Key outcomes of interlayer contact engineering

The statistical analysis of 160 FETs demonstrates that the incorporation of a monolayer MoS_2 UCI has a profound impact on WS_2 device performance. Although the Schottky barrier height was not explicitly measured, reduction in contact resistance – exceeding 60% at typical

operating carrier concentrations – strongly indicates that the UCI effectively lowers the barrier at the metal–semiconductor interface. This reduction directly translates into higher field-effect mobility, increased ON-state current and I_{ON}/I_{OFF} ratio, lower threshold voltage and improved SS. Importantly, the observed trends are highly reproducible across multiple devices, emphasizing the robustness of the Au/MoS_2/WS_2 design and confirming that careful interface engineering can systematically tune the Fermi level pinning effect. Equally important is the methodology itself: by employing a gold-assisted transfer of pre-patterned MoS_2 interlayers, the need for selective etching of the monolayer on top of another 2D material was eliminated. This approach, originally developed specifically to enable the placement of atomically thin under-contact interlayers, provides a reliable and non-destructive alternative to conventional etching-based techniques. By avoiding direct patterning of MoS_2 on WS_2, it preserves channel integrity, reduces the risk of defect introduction, and simplifies the fabrication flow, thereby demonstrating a clean and reproducible route for implementing van der Waals contacts. These findings underscore the potential of the van der Waals interlayer approach as a versatile strategy in 2D FET contact engineering, enabling both improved performance and enhanced uniformity.

It should be emphasized, however, that the contact resistance values obtained in this study are not record-low when compared to the best reports in the literature[95]. This outcome is not unexpected, since the primary objective here was not to surpass state-of-the-art benchmarks but rather to explore the challenge of high contact resistance from a different angle and to demonstrate how interlayer engineering can modify band alignment and mitigate Fermi level pinning at metal–semiconductor junctions. Nevertheless, there are strong indications that further optimization of interface cleanliness could enable this approach to reach even lower resistance values. In particular, avoiding contamination associated with transfer processes - such as by employing selective growth methods for 2D heterostructures - may provide much cleaner interfaces. In this context, it is worth noting recent work[154], to which I also contributed as a co-author, demonstrating that selective epitaxial growth of van der Waals heterostructures can yield atomically sharp and uncontaminated junctions. If such approaches could be extended to other 2D material combinations, the interlayer concept introduced here may be pushed to record-level contact performance.

Beyond the improvements in individual performance metrics, this study highlights the value of statistical validation in evaluating contact engineering approaches. By analyzing a large device population rather than isolated examples, the results provide a realistic picture of variability and demonstrate that the benefits of the MoS_2 interlayer are consistently expressed across the entire

dataset. Such statistical robustness is crucial when assessing strategies intended for scalable electronics, as it ensures that the observed improvements are not artifacts of a few exceptional devices.

In addition, the methodology established here can be readily extended to other TMD systems and alternative interlayer materials, offering a generalizable framework for tailoring metal - semiconductor interfaces through van der Waals engineering. This flexibility broadens the relevance of the approach beyond the specific Au/MoS_2/WS_2 system studied. Finally, future work focused on interfacial cleanliness, dielectric integration, and large-area synthesis could further amplify the advantages of such designs, bringing interlayer-based contact engineering closer to practical implementation in 2D CMOS technologies.

Chapter 6. Gate dielectric integration enabled by vdW metal seed layers in 2D FETs

The results presented in this chapter are part of a manuscript entitled 'Integration of high-κ gate dielectrics with 2D semiconductors via self-oxidizing vdW metal seed layers', which has been submitted to a peer-reviewed journal. I am listed as a co-first author of this work.

6.1. Issues with ALD on pristine 2D semiconductors

For 2D transistors to compete with advanced silicon technology, they must be integrated with ultrathin high-κ dielectrics that provide strong electrostatic control, suppress short-channel effects, and minimize gate leakage at deeply scaled nodes *(High-k dielectric integration on 2D materials*). However, direct ALD on pristine 2D semiconductors is fundamentally hindered by their chemically inert surfaces. Unlike conventional substrates, 2D crystals lack dangling bonds or reactive groups, leaving ALD precursors unable to nucleate uniformly. As a result, dielectrics deposited directly on bare monolayers grow discontinuously, forming rough, island-like films with pinholes that lead to poor reliability and excessive leakage currents.

Several strategies have been attempted to overcome this nucleation problem. Surface treatments[59,72] introduce artificial nucleation sites but also damage or dope the channel. Modified ALD processes and special precursors[70,155] improve coverage at the expense of material quality. Thin buffer/seeding[71,156] layers promote nucleation but add parasitic thickness and often trap charges. Alternatively, transferred 2D dielectrics[76,157,158] such as offer clean interfaces but suffer from low permittivity and limited scalability. Despite extensive efforts, no general CMOS-compatible solution exists for conformal, high-κ dielectric growth on 2D semiconductors. This motivates the search for alternative seeding strategies that both enable uniform ALD nucleation and preserve the intrinsic properties of the 2D channel.

6.2. Oxidation behavior of vdW metals and seed layer formation

Given the difficulties of direct ALD on pristine 2D semiconductors, an alternative strategy was explored here: the use of van der Waals metals that naturally oxidize into insulating layers, which can serve as effective seed layers for subsequent high-κ dielectric deposition.

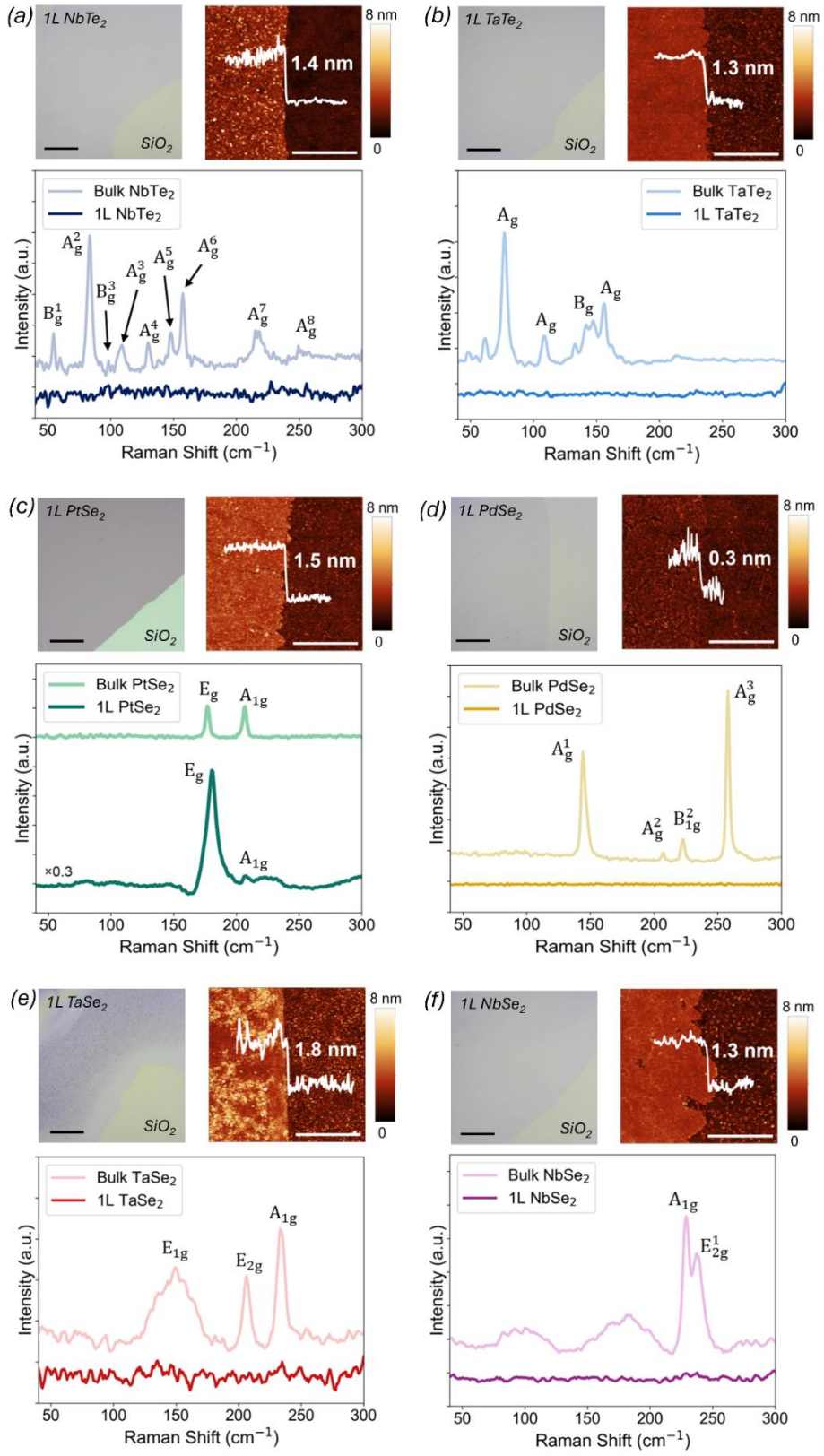

Figure 34 *(Top left) Optical images of exfoliated monolayer flakes. (Top right) AFM height maps of the monolayers. (Bottom) Raman spectra comparing monolayer and bulk flakes of* ***(a)*** *$NbTe_2$,* ***(b)*** *$TaTe_2$,* ***(c)*** *$PtSe_2$,* ***(d)*** *$PdSe_2$,* ***(e)*** *$TaSe_2$, and* ***(f)*** *$NbSe_2$. Scale bars on optical images are 50 µm. Scale bars on AFM images are 500 nm. Measurements were performed using Bruker Dimension Icon AFM and Horiba MacroRAM Raman system.*

Certain layered metallic dichalcogenides have been found to oxidize spontaneously, forming uniform insulating films. Layered crystals of $TaSe_2$, $NbTe_2$, $PtSe_2$, $PdSe_2$, $TaTe_2$, $NbSe_2$, when exfoliated and exposed to air, convert into ultrathin oxides with pinhole-free coverage.

Figure 34 shows optical and AFM images of six monolayers of tellurides and selenides fabricated using gold-assisted exfoliation on SiO_2/Si substrates; AFM confirms nominal monolayer thickness, although the apparent height is slightly larger due to oxidation-induced volume expansion, a phenomenon previously reported in other layered materials[159]. Raman spectroscopy (**Figure 34**) further reveals that bulk crystals have sharp phonon peaks, consistent with the typical Raman features reported for $TaSe_2$[160], $NbTe_2$[161], $PtSe_2$[162], $PdSe_2$[163], $TaTe_2$[164], and $NbSe_2$[165]. In contrast, the corresponding monolayers show complete quenching of those modes – a clear sign of chemical transformation, except for $PtSe_2$, which retains its Raman signature, suggesting a slower or qualitatively different oxidation process compared to the other metallic TMDs.

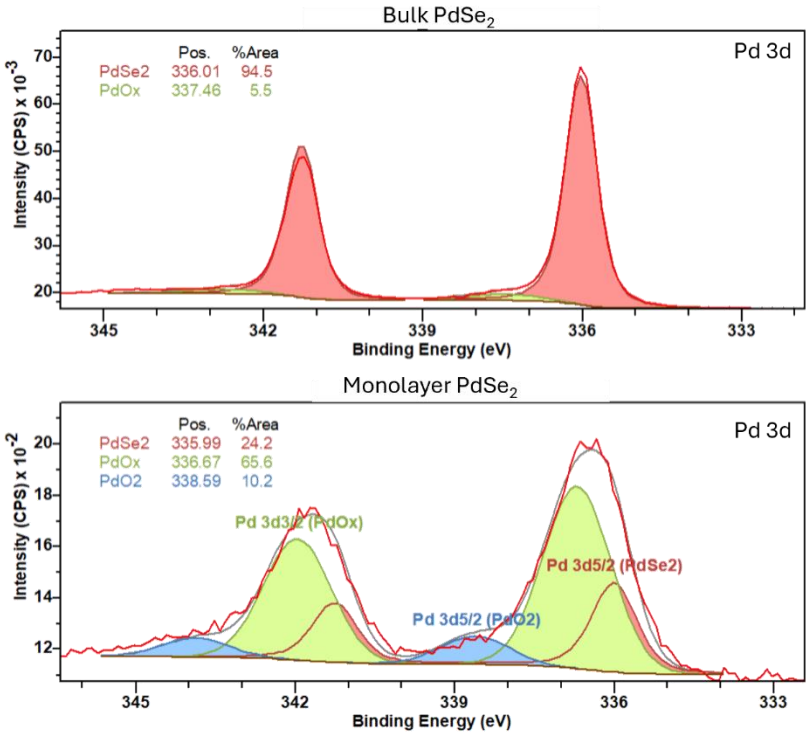

Figure 35 *XPS obtained for bulk and monolayers of $PdSe_2$. The experimental data shown in this figure were acquired and analyzed by Bob Hengstebeck from the Pennsylvania State University.*

X-ray photoelectron spectroscopy substantiates this picture: all monolayer vdW metals show metal–oxide and chalcogen–oxide peaks after ambient exposure, whereas the bulk crystals retain purely metallic spectra. XPS of the representative seed layer ($PdSe_2$) shows clear oxide-

related features in core levels of monolayer, while the corresponding bulk crystal retains metallic spectra (**Figure 35**). This indicates that oxidation is primarily restricted to the monolayer due to their large surface-to-volume ratio. Although comparable oxidation features were observed in the monolayers of all six seed materials, only $PdSe_2$ is presented here, since the full analysis of the remaining datasets is extensive and lies beyond the scope of this thesis.

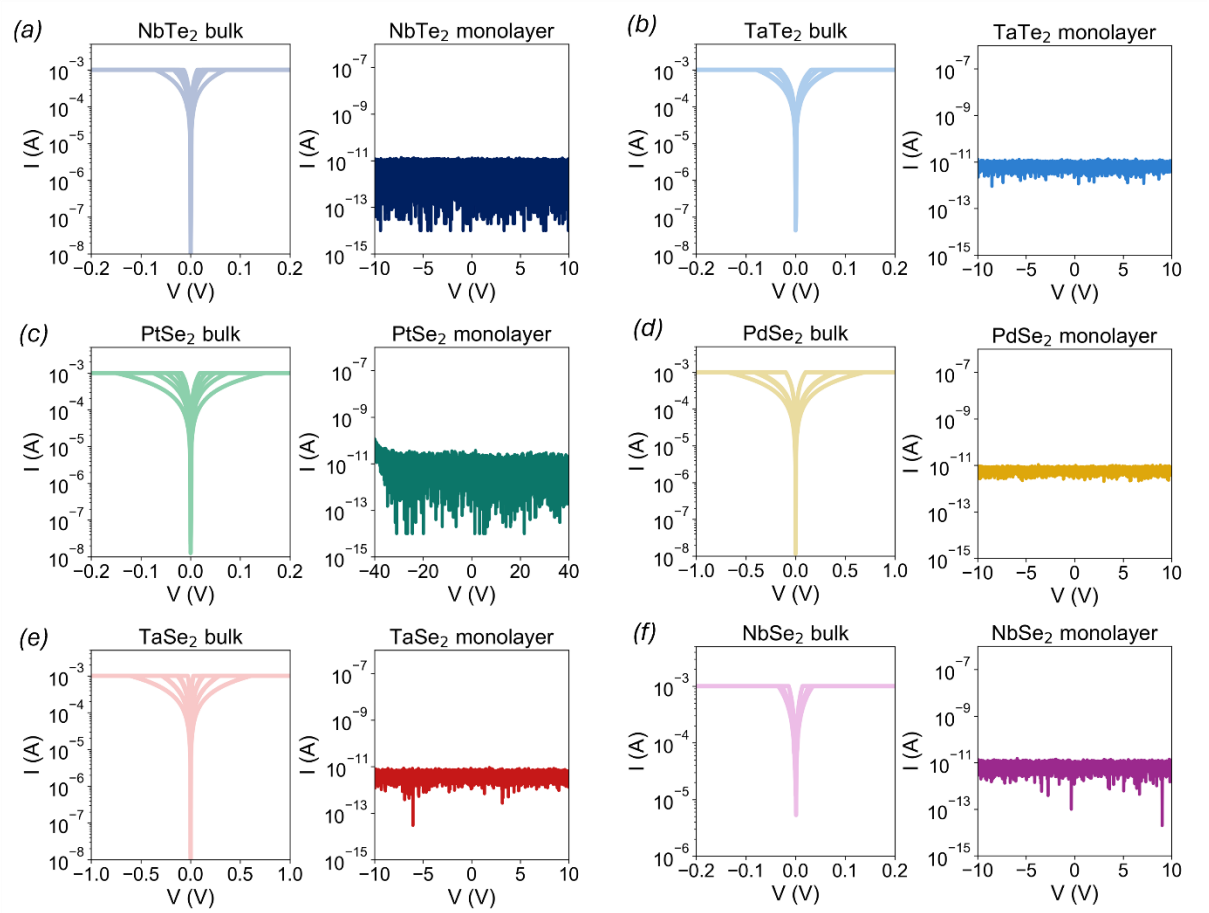

Figure 36 *Current–voltage (I–V) plots for (left) bulk and (right) monolayer flakes of* ***(a)*** *$NbTe_2$,* ***(b)*** *$TaTe_2$,* ***(c)*** *$PtSe_2$,* ***(d)*** *$PdSe_2$,* ***(e)*** *$TaSe_2$, and* ***(f)*** *$NbSe_2$. For bulk flakes, a high current is observed even at low bias voltages, whereas for monolayers, no signs of conductivity are detected even at higher applied voltages.*

Having established the formation of native oxides in monolayers, their influence on electronic transport was next examined. Crucially, those oxidized monolayers are highly insulating. For transport characterization, contacts were defined using standard photolithography (Heidelberg MLA150 Direct Write Lithography system), followed by electron beam evaporation of Pt/Pd (20/13 nm) contacts on top of each of the six materials in both bulk and monolayer forms. Two-terminal transport measurements (**Figure 36**) show that bulks are metallic, whereas the oxidized monolayer versions conduct currents in the picoampere range. In other words, each monolayer metal undergoes a metal-to-insulator transition upon oxidation.

6.3. Seed-layer-assisted growth of high-κ dielectrics

To assess the viability of oxidized vdW metals as seed layers for dielectric integration, test structures were designed to mimic the target device geometry, in which a semiconductor channel lies beneath the seed layer. Monolayer WSe_2 was first prepared using gold-assisted exfoliation onto a SiO_2/Si substrate, followed by gold-assisted exfoliation of a monolayer vdW seed layer on top. Upon ambient exposure, the metallic layer spontaneously oxidized, and subsequently, a 5 nm HfO_2 film was deposited by ALD at 150 °C.

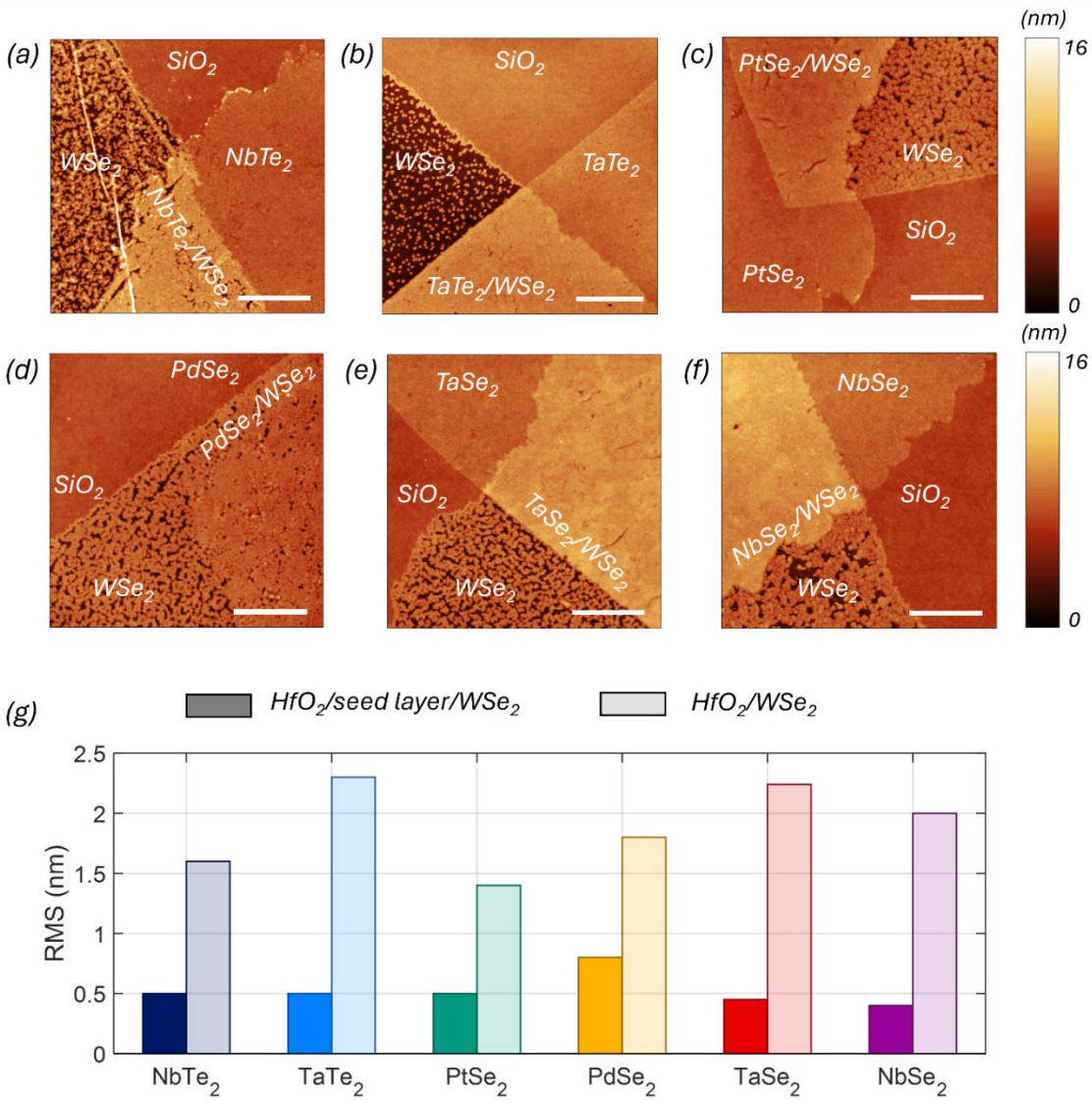

Figure 37 *AFM scans depicting the surface morphology of 5 nm HfO_2 grown by ALD on four regions: bare SiO_2, bare WSe_2, seed layer on SiO_2, and seed layer on WSe2, for monolayers of* ***(a)*** *$NbTe_2$,* ***(b)*** *$TaTe_2$,* ***(c)*** *$PtSe_2$,* ***(d)*** *$PdSe_2$,* ***(e)*** *$TaSe_2$, and* ***(f)*** *$NbSe_2$. Scale bars are 500 nm.* ***(g)*** *RMS roughness values of 5 nm HfO_2 extracted from AFM data, comparing growth on bare WSe_2 and on WSe_2 covered with seed layers.*

The resulting samples contained regions of bare WSe_2, bare seed layers, and WSe_2 capped with a seed layer, all uniformly covered with HfO_2. AFM imaging (**Figure 37a–f**) was then employed to assess the dielectric morphology. Across all measured regions, the HfO_2 surface on oxidized seed layers is markedly smoother than that on bare WSe2, where nucleation is sparse and produces island-like, rough patches. On oxidized vdW seed layers the HfO_2 films are continuous, with only occasional small discontinuities. In particular, $TaTe_2$, $TaSe_2$, $PdSe_2$, and $NbSe_2$ provide excellent dielectric coverage, highlighting the effectiveness of these materials as seeding layers for uniform high-κ deposition.

Quantitatively, the RMS roughness of the HfO_2 film decreases from ≳1.5 nm on seedless WSe_2 to <0.5 nm on vdW-seeded regions (**Figure 37g**). This dramatic improvement indicates that even a single monolayer of oxidized vdW metal uniformly overcomes the ALD nucleation barrier.

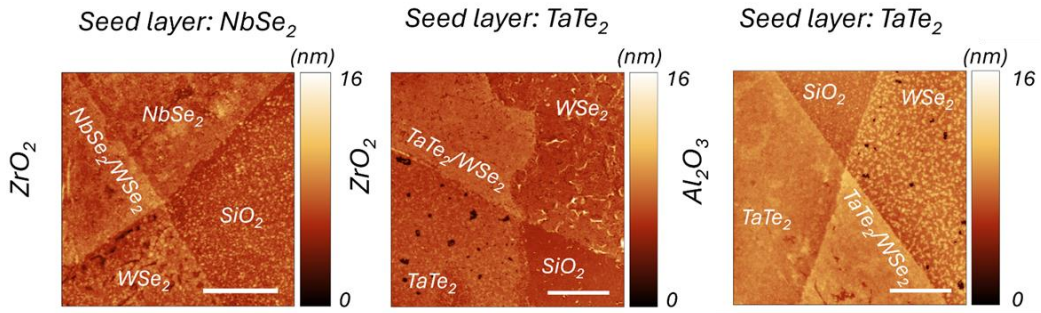

Figure 38 *AFM scans showing the surface topographies of Al_2O_3 and ZrO_2 films grown on bare SiO_2, monolayer WSe_2, and oxidized van der Waals seed layers ($NbSe_2$ and $TaTe_2$).*

Moreover, this behavior is not limited to HfO_2: similarly uniform coverage of Al_2O_3 and ZrO_2 films on WSe_2 was also observed when $NbSe_2$ or $TaTe_2$ monolayers were employed as seed layers (**Figure 38**). While growth on bare WSe_2 was patchy and non-uniform, the oxidized seed layers consistently enabled smooth, pinhole-free dielectric films. These results demonstrate that oxidized vdW metal monolayers act as general nucleation promoters for a variety of high-κ oxides on 2D semiconductors.

6.4. Breakdown characteristics, dielectric properties, and frequency response

The dielectric reliability of HfO_2 films deposited on vdW seed layers was evaluated using MIM capacitor structures. Each capacitor comprised a Pt/Ti (15/5 nm) bottom electrode, a single monolayer of oxidized vdW seed layer, a 5 nm HfO_2 layer, and a Pt/Pd (13/20 nm) top electrode, as schematically shown in **Figure 39a**. The overlap area between the electrodes was fixed at

200 nm × 1 μm to ensure consistent device geometry. Prior to dielectric deposition, the vdW monolayers were exposed to a mild ozone treatment for two minutes to remove surface contaminants. HfO_2 was subsequently deposited by ALD at 150 °C. It should be emphasized that ozone treatment step was introduced only during the fabrication of MIM capacitors and subsequent devices. It was not applied to samples used for XPS, Raman, or conductivity measurements that probed the intrinsic oxidation behavior of the seed layers. Therefore, the analysis of their chemical and electronic transformation from metallic to insulating states remains unaffected by this step. Nevertheless, ozone exposure may assist the oxidation process during device fabrication, although it is not considered the primary factor driving the transformation of the seed layers.

Breakdown voltage was measured on ~30 devices for each seed layer. **Figure 39b-h** shows current density–voltage curves. Breakdown voltages (V_{BR}) were extracted as voltages at which a sharp increase of current was visible. Weibull analysis (**Figure 39i**) was performed using the standard Weibull failure relation described by **Equation 26**:

$$F(E_{BR}) = 1 - \exp\left[-\left(\frac{E_{BR}}{E_{\mu}}\right)^{k}\right] \qquad \textbf{Equation 26}$$

$$E_{BR} = \frac{V_{BR}}{d} \qquad \textbf{Equation 27}$$

where E_{BR} is the breakdown field, k is the shape parameter and E_{μ} is the scale parameter corresponding to the mean breakdown field (E_{BRM}) and mean breakdown voltage V_{BRM}. Structures yield median breakdown voltages of roughly ±5 V or higher (**Figure 39j**), corresponding to electric fields in most cases higher than 5 MV/cm. For instance, capacitors seeded with $TaTe_2$ or $TaSe_2$ reached breakdown around –5.4 V under negative bias, while for positive bias, those with $PtSe_2$ reached near +5.0 V. Control devices without any seed layer showed breakdown at –5.0 V and +5.5 V, indicating that the incorporation of a vdW oxide does not compromise the intrinsic dielectric strength of HfO_2.

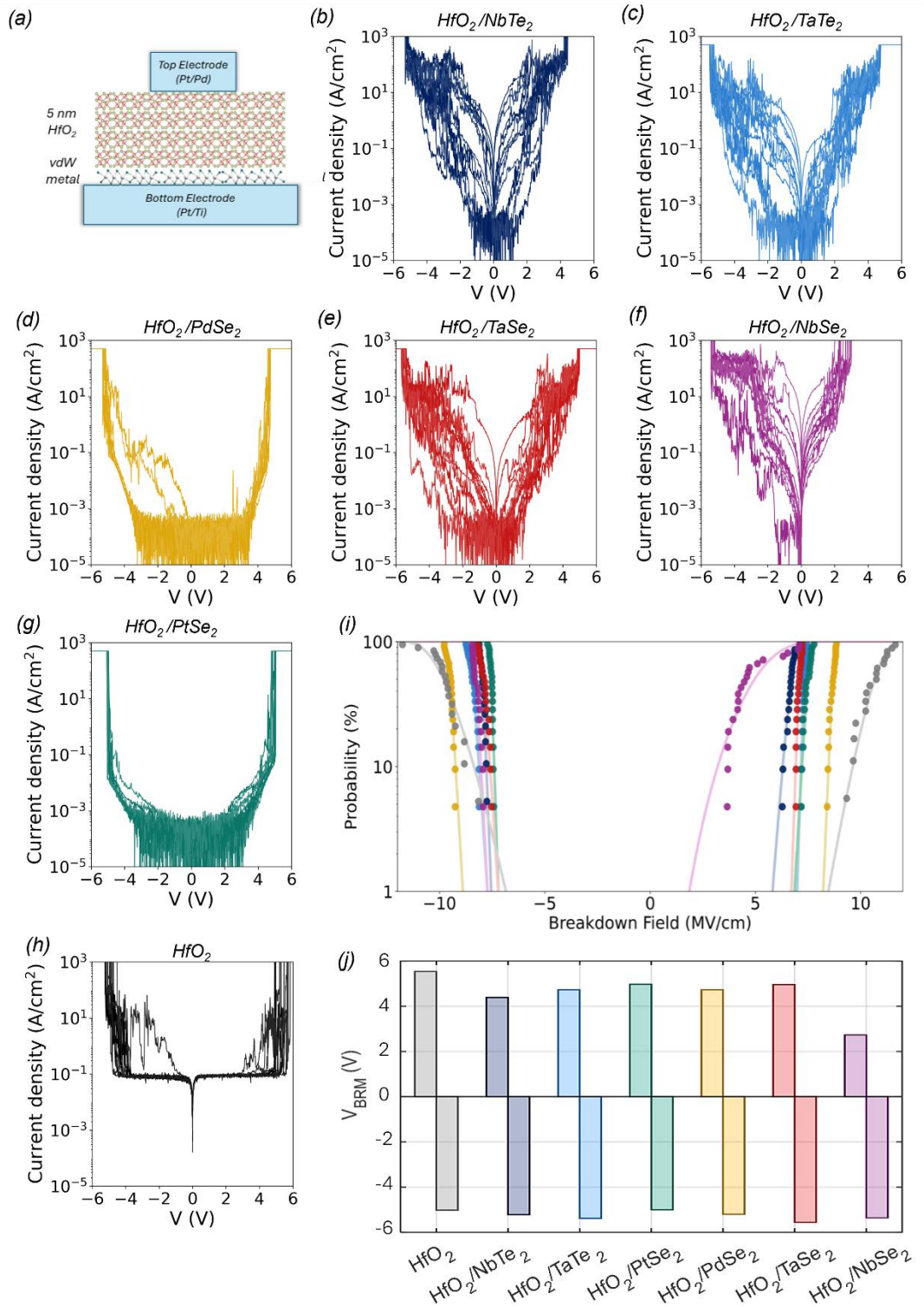

Figure 39 (a) *Schematic illustration of the MIM capacitor structure consisting of a Pt/Ti bottom electrode, a monolayer vdW seed layer, a 5 nm HfO_2 dielectric, and a Pt/Pd top contact. Current density–voltage characteristics from more than 30 devices for* ***(b)*** *$HfO_2/NbTe_2$,* ***(c)*** *$HfO_2/TaTe_2$,* ***(d)*** *$HfO_2/PtSe_2$,* ***(e)*** *$HfO_2/PdSe_2$,* ***(g)*** *$HfO_2/TaSe_2$,* ***(g)*** *$HfO_2/NbSe_2$ and* ***(h)*** *HfO_2.* ***(i)*** *Cumulative breakdown field distributions with Weibull fits for 5 nm HfO_2 grown on different vdW seed layers. Colors correspond to seed layer on previous graphs on this figure.* ***(j)*** *Bar chart summarizing the mean breakdown voltages (V_{BRM}) extracted from Weibull analysis.*

Moreover, the Weibull distributions indicate not only high breakdown fields but also narrow variability, underscoring the reproducibility of this approach. Furthermore, with the exception of $NbSe_2$, all seeded devices satisfied the International Roadmap for Devices and Systems (IRDS) target for advanced gate insulators, which requires leakage current densities below 10^{-2} A cm^{-2} at 1 V[166]. Here, the leakage current refers to the small residual current flowing through the dielectric before the sharp increase associated with breakdown; in practice, it was determined from the current density–voltage characteristics as the current preceding the breakdown event (**Figure 39b-h**), and it consistently remained below the IRDS threshold. These results confirm that oxidized vdW monolayers enable uniform high-κ deposition while preserving dielectric integrity, making them a viable route for integrating ultrathin gate stacks in 2D electronics.

Next, for capacitance measurements, large-area MIM capacitor structures were fabricated on Si substrates. First, a uniform Pt/Ti (15/5 nm) bottom electrode was deposited across the wafer by electron beam evaporation, followed by gold-assisted exfoliation of monolayer seed layers, mild ozone treatment, and deposition of 25 nm of HfO_2 to minimize leakage. Square capacitor pads of various lateral dimensions (40 × 40 μm, 60 × 60 μm, 80 × 80 μm, and 100 × 100 μm) were then defined by standard photolithography, Finally, Pt/Pd (20/13 nm) was deposited as the top electrode, completing the metal–insulator–metal geometry.

Capacitance measurements on these MIM structures enabled evaluation of the effective dielectric constant (k_{eff}) of the combined vdW seed layer/HfO_2 stack. As expected for dielectrics with uniform properties, the measured capacitance scaled linearly with device area (**Figure 40a**) following the **Equation 22**. From this scaling, κ_{eff} values were extracted and found to be similar to those of HfO_2 alone (**Figure 40b**), indicating that the high bulk dielectric constant of HfO_2 (~16) is preserved despite the presence of the ultrathin vdW oxide at the interface. In other words, the seed layer does not compromise the stack capacitance.

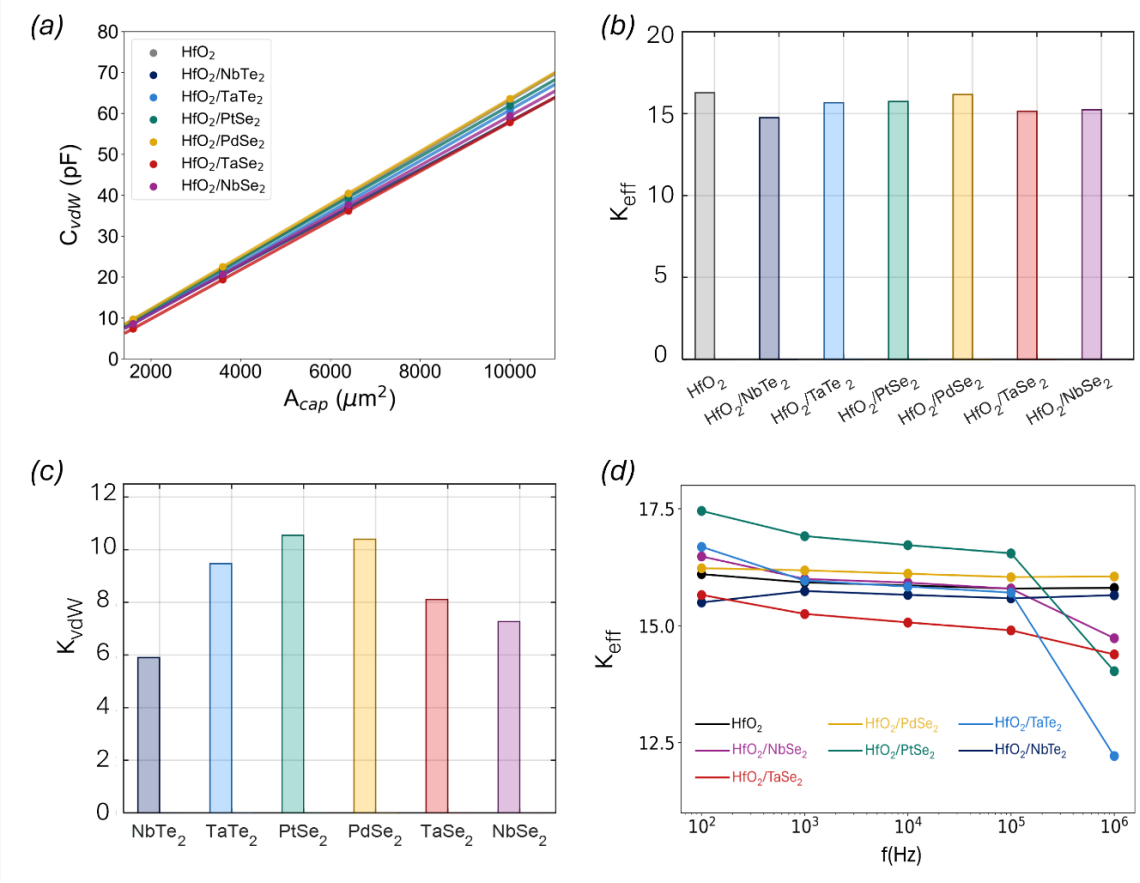

Figure 40 (a) *Capacitance (C_{vdW}) as a function of capacitor area (A_{cap}) for MIM devices incorporating 25 nm-thick HfO_2 deposited on oxidized monolayer vdW seed layers,* ***(b)*** *Extracted effective dielectric constants (κ_{eff}) of HfO_2 films drown with different seed layers,* ***(c)*** *Dielectric constants (κ_{vdW}) of the interfacial seed layers, extracted by modeling the vdW/HfO_2 stack as two capacitors in series and isolating the seed layer contribution.* ***(d)*** *Frequency-dependance of effective dielectric constant.*

To probe the dielectric contribution of the seed layer itself, the system was modeled as a series combination of two capacitors: 25 nm HfO_2 film and vdW seed layer. This analysis revealed that all self-oxidized seed layers exhibit remarkably high intrinsic dielectric constant κ_{vdW} (**Figure 40c**), substantially exceeding those of conventional interfacial layers typically used in ALD seeding[61,167,168]. This is a particularly important advantage: while conventional low-κ buffers dilute the total gate capacitance, the vdW oxides, being both ultrathin and exhibit high dielectric constant, maintain or even enhance the electrostatic efficiency of the gate stack.

The electrical integrity of these dielectrics was further validated by frequency-dependent capacitance measurements. Capacitance values remained highly stable, with less than 5% variation across the frequency range from 100 Hz to 1 MHz (**Figure 40d**). Such minimal dispersion indicates that the gate stacks exhibit a low density of interface traps and negligible

dielectric relaxation effects, both of which are crucial for reliable high-frequency transistor operation.

Taken together, the measured breakdown strength, dielectric constant values, and minimal frequency dispersion confirm that gate stacks incorporating oxidized vdW seed layers possess excellent dielectric quality. These seed layers not only resolve the intrinsic ALD nucleation barrier on 2D semiconductors but also contribute positively to the electrical integrity of the resulting HfO_2 films. The results strongly suggest that these dielectric stacks could be well-suited for top-gate integration in 2D FETs, a possibility that is further explored in the following subchapter.

6.5. Top-gated 2D FETs using vdW metal seed layers

To directly assess the device-level advantages of vdW-seed-layer-assisted high-κ dielectric integration, dual-gated monolayer FETs were fabricated using large-area MOCVD-grown WSe_2 bilayer and MoS_2 monolayer as p- and n-type channels, respectively. A schematic illustration of the device structure is presented in **Figure 41a**. The local back gates for WSe_2 FETs consisted of patterned using electron beam lithography (Vistec Litography system) and electron beam deposited Pt/Ti (15/5 nm) gate islands on SiO_2/Si substrate, covered by a 10 nm HfO_2 back-gate dielectric grown by ALD. For MoS_2 devices, a global back-gate configuration was employed, in which Pt/Ti (15/5 nm) layer was deposited across the entire SiO_2/Si substrate and capped with a 25 nm ALD-grown HfO_2 layer. Onto these back-gated platforms, the 2D channel layers were transferred from a sapphire substrate using a PMMA-assisted method[105]. The channels were subsequently patterned with electron beam lithography and etched, follow by source and drain contact electron-beam deposition: Ni/Pt/Ni (30/20/10 nm) stacks for MoS_2 and Pt/Pd (12/13 nm) stacks for WSe_2. A post-fabrication NO doping step was applied to WSe_2 devices (100 °C, 30 min) to promote stable p-type conduction.

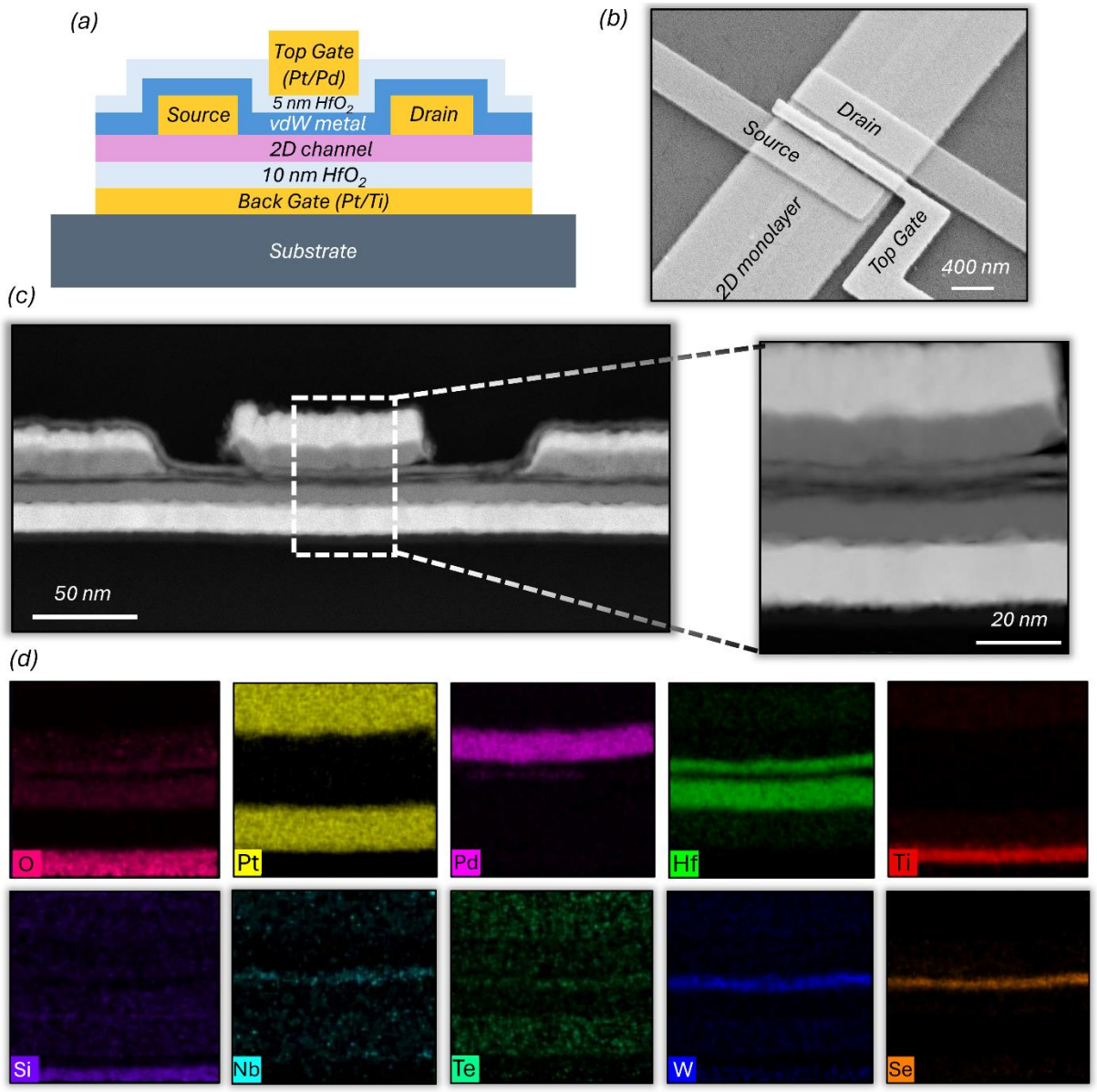

Figure 41 (a) *Schematic illustration and* ***(b)*** *SEM image of a dual-gated 2D FETs, where self-oxidizing vdW metal seed layers enable ALD deposition of a 5 nm HfO_2 top-gate dielectric.* ***(c)*** *Cross-sectional TEM image of a WSe_2 FET and* ***(d)*** *the corresponding EDX elemental map of the region marked in panel* ***(c)****, demonstrating the use of an $NbTe_2$ seed layer. TEM and EDX experimental data shown in this figure were acquired and analyzed by Lei Ding from the Pennsylvania State University.*

Following the definition of the base back-gated devices, monolayers of vdW metals ($TaSe_2$, $TaTe_2$, $NbSe_2$, $NbTe_2$, $PdSe_2$, $PtSe_2$) were exfoliated with gold-assisted method directly onto the semiconductor channels to serve as self-oxidizing seed layers. Mild ozone treatments were applied (2–3 min, depending on the material) to further clean the surface. Subsequently, a 5 nm HfO_2 top-gate dielectric was deposited by ALD at 150 °C. Finally, Pt/Pd top-gate electrodes (13/20 nm) were deposited, with gate lengths of 100 nm for WSe_2 devices (channel length in all devices was 290 nm) and 300 nm for MoS_2 devices (channel length in devices with $TaSe_2$ –

1100 nm, with $TaTe_2$ – 425 nm), completing the dual-gated FET architecture. Devices based on WSe_2 were fabricated using all six seed layer materials, whereas MoS_2 devices were realized only with two seed layers ($TaSe_2$ and $TaTe_2$). SEM images of representative devices (**Figure 41b**) and cross-sectional TEM combined with EDX mapping (**Figure 41c,d**) of representative devices with $NbTe_2$ seed layer confirmed the intended material stacking. In particular, Nb and Te signals verified the successful inclusion of $NbTe_2$ seed layer, while W and Se signatures identified the underlying WSe_2 channel.

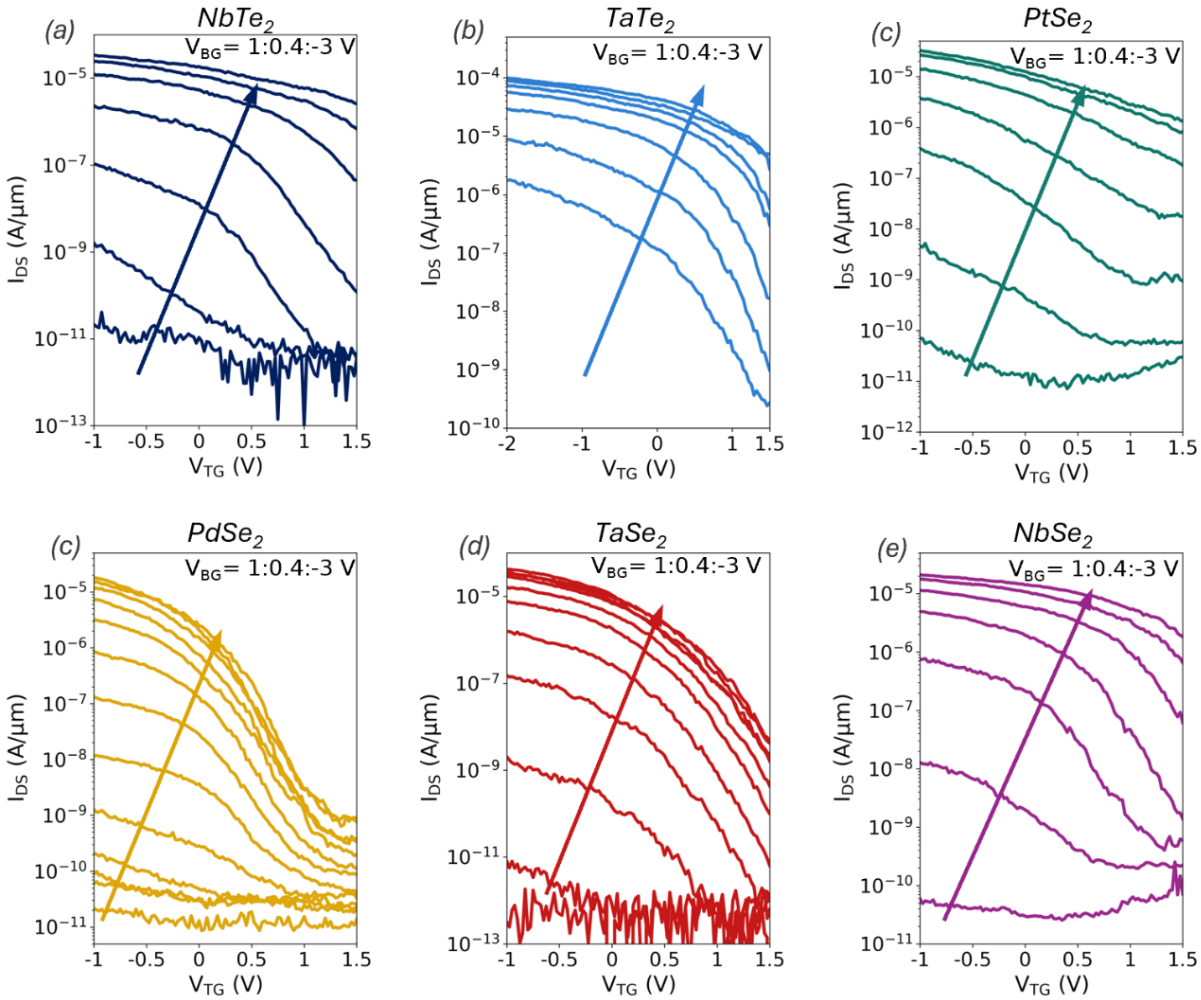

Figure 42 *Dual-gate transfer characteristics of p-type WSe_2 FETs using* ***(a)*** *$NbTe_2$,* ***(b)*** *$TaTe_2$,* ***(c)*** *$PtSe_2$,* ***(d)*** *$PdSe_2$,* ***(e)*** *$TaSe_2$ and* ***(f)*** *$NbSe_2$ seed layers. In all measurements V_{DS} = -1 V.*

Top-gate transfer characteristics of p-type WSe_2 FETs incorporating all seed layers are presented in **Figure 42a-f**. When sweeping top-gate voltage (V_{TG}) from –1 V to +1.5 V while stepping V_{BG} between -3 V to near 0 V values, the highest ON-currents were observed under simultaneous negative biasing of both gates. Here, the back gate influences both the channel and contact regions, modulating the Schottky barrier width at the source/drain junctions, while

the top gate primarily controls the channel segment. This complementary action ensures that the back gate primarily governs the ON-state characteristics, whereas the top gate plays a decisive role in managing the OFF-state, yielding ON/OFF ratios above 10^5 and subthreshold slopes down to 151 mV/dec.

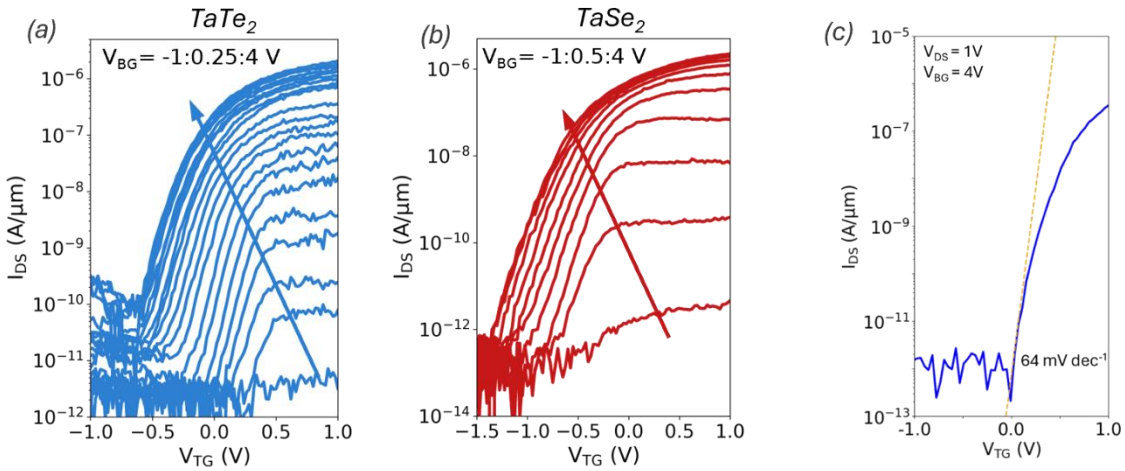

Figure 43 *Dual-gate transfer characteristics of n-type MoS_2 FETs using* ***(a)*** *$TaTe_2$ and* ***(b)*** *$TaSe_2$ seed layer.* ***(c)*** *Extraction of SS from transfer characteristics of device with $TaTe_2$ seed layer. In all measurements V_{DS} = 1 V.*

Analogous behavior was observed for n-type MoS_2 devices incorporating $TaTe_2$ and $TaSe_2$ seed layers (**Figure 43a,b**). With V_{TG} swept between –1 V and +1 V and V_{BG} stepped between –1 V and +4 V, the strongest conduction occurred under simultaneous positive biasing of both gates. Device with $TaSe_2$ seed layers exhibited superior ON/OFF ratios exceeding 10^7, whereas the one with $TaTe_2$ provided steeper subthreshold slopes. In particular, a $TaTe_2$-based device with the channel length of 5 μm reached 64 mV/dec at V_{DS} = 1 V, showing exceptional gate control (**Figure 43c**).

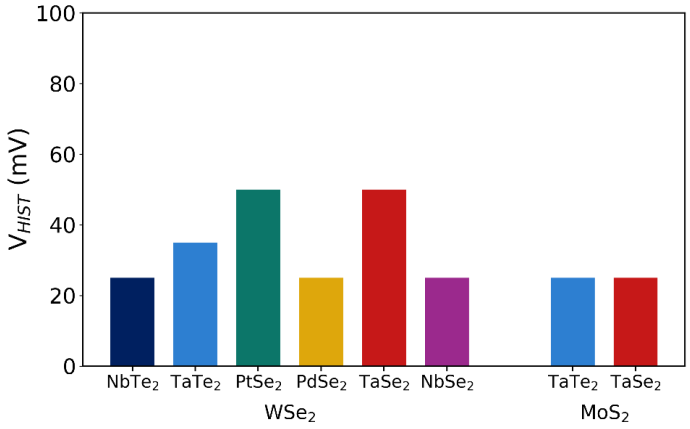

Figure 44 *Extracted hysteresis values (V_{HIST}) for different seed layers used in WSe_2 and MoS_2 devices.*

It is important to note that SS strongly depends on channel length and thus top gate length: long-channel devices enable near-ideal slopes close to the thermionic limit (60 mV/dec), while shorter channels inherently suffer from stronger electrostatic degradation. Remarkably, while most reports approaching this limit rely on micron-scale gate lengths[61,71,169], the presented devices achieve excellent electrostatics even with 300 nm-long gates.

Moreover, dual-sweep measurements revealed hysteresis (**Figure 44**) going down to 25 mV, confirming that the dielectric/semiconductor interfaces remain clean and nearly trap-free. A particularly noteworthy aspect of this device architecture is the dual nature of the vdW seed layers. At the seed layer/2D semiconductor interface, the channel remains coupled to the seed layer only through the van der Waals interactions, which preserves the intrinsic semiconductor properties. At the exposed surface, however, spontaneous oxidation of the metallic monolayer transforms it into a chemically active layer that provides abundant nucleation sites for ALD. This combination of an inert channel interface with an activated dielectric interface underpins the ability to achieve conformal high-κ integration without compromising the quality of the underlying 2D semiconductor channel in top-gated devices.

6.6. Concluding discussion on gate stack engineering

The results presented in this chapter demonstrate that self-oxidizing vdW metal monolayers can act as effective seed layers for the integration of ultrathin high-κ dielectrics on 2D semiconductors. Their spontaneous oxidation yields atomically thin, uniform insulators that overcome the intrinsic ALD nucleation barrier, enabling conformal growth of HfO_2 and other dielectrics on otherwise inert surfaces. Importantly, these vdW seed layer/HfO_2 stacks exhibit remarkable dielectric properties as reflected by high breakdown fields, stable capacitance scaling, and minimal frequency dispersion, while their dielectric constant remains in the high-κ range. Device integration further showed that dual-gated WSe_2 and MoS_2 transistors fabricated with these stacks exhibit strong gate control, steep subthreshold slopes, low hysteresis, and competitive on/off ratios, confirming that the method provides a viable route to functional 2D FETs.

At the same time, the study was primarily focused on exploring the problem of dielectric integration and interfacial engineering, rather than maximizing device benchmarks, yet the devices achieved demonstrate performance metrics of high quality. To establish the full potential of vdW seed layers, future work must involve statistical studies across larger device populations for both n- and p-type channels, providing a reliable picture of performance

distributions and variability. It will also be important to rigorously verify whether the oxidized monolayers are electrically neutral or whether they introduce any degree of charge transfer doping to the underlying semiconductors, an issue that has been problematic for conventional seed layers. Addressing these points will be essential to confirm that the observed improvements are both reproducible and intrinsic. The present study highlights a promising pathway toward scalable gate stack engineering in 2D electronics, tackling the long-standing challenge of dielectric integration while laying the groundwork for future optimization and broader application.

Chapter 7. Conclusions

7.1. Summary of key results

In this dissertation, a multifaceted approach was adopted to explore critical challenges in 2D FETs, focusing on solving manufacturing challenges in achieving high-quality 2D layers, contacts, and gate dielectrics by understanding their underlying operation and the key factors that influence them (surface cleanliness, band alignment, nucleation processes). While the primary demonstration is on 2D FETs, the work advances the interface engineering of van der Waals materials, which is broadly relevant not only to nanoelectronics but also to fields such as optoelectronics[170,171] and photonics[172], as well as sensing and bioelectronics[173], all of which seek to exploit the unique properties of 2D materials.

A gold-assisted exfoliation technique was first optimized to obtain large-area monolayer MoS_2 and WSe_2 flakes, enabling fabrication of extensive device arrays. Using this method, 120 n-channel (MoS_2) and 120 p-channel (WSe_2) FETs were produced, providing a broad statistical dataset for performance evaluation. Notably, the WSe_2 transistors represent the first successful demonstration of p-type devices fabricated with this gold-assisted approach. The monolayer devices exhibited competitive electrical characteristics: median on-currents on the order of 40–50 μA/μm (with best value of 88 μA/μm for p-FET and 63 μA/μm for n-FET) and high on/off current ratios (~10^7–10^8). Subthreshold swing values down to ~85–102 mV/dec were achieved in the best devices, indicating effective channel electrostatic control. These results, which approach the performance of the best CVD-grown monolayer devices, confirm that the gold-assisted method can isolate large-area monolayers without compromising device quality. This work also demonstrated CMOS logic circuits based on monolayer 2D semiconductors. By pairing MoS_2 n-FETs with WSe_2 p-FETs, functional CMOS inverters were constructed and evaluated. The inverters showed full rail-to-rail switching, symmetric transfer curves with switching thresholds and fast transient response, all achieved at low supply voltages (1–3 V). Notably, these monolayer CMOS inverters exhibited minimal static power dissipation (~50-80 pW at V_{DD}=3 V) due to low off-state leakage of the 2D FETs. The measured propagation delays were also low and compared favorably with prior 2D inverter demonstrations. The study demonstrates that gold-assisted exfoliation is a powerful tool for preparing high-quality monolayers. Crucially, optimizing this technique required understanding the exfoliation mechanics and surface interactions to ensure layer integrity and minimize defects. While the method delivers device-grade layers, its reliance on manual exfoliation and multiple cleaning

steps makes it more suitable for research and prototyping than for large-scale industrial applications.

The second focus of this work addressed the pervasive issue of high contact resistance in 2D FETs through ultrathin contact interlayer engineering. This strategy was informed by a detailed understanding of how Fermi-level pinning and band alignment at the metal/semiconductor interface impact contact resistance. A monolayer MoS_2 under-contact interlayer was inserted at the metal/semiconductor interface of WS_2 transistors, forming an engineered Au/MoS_2/WS_2 junction. This stack was designed to mitigate Fermi-level pinning and lower the Schottky barrier for carrier injection. Comprehensive statistical measurements on 160 devices – half with the MoS_2 interlayer and half without – showed that the interlayer yields significant performance gains. In devices with the MoS_2 interlayer, the extracted contact resistance was reduced by over 60%. This dramatic reduction in R_c directly translated into higher on-state currents, improved field-effect mobilities, and lower threshold voltages compared to control devices. Importantly, these improvements were highly reproducible across the entire device population, underscoring the robustness of the approach. The data showed that even at longer channel lengths, interlayer devices became truly channel-limited (with contact resistance contributing only a minor fraction of total resistance), whereas in control devices the contacts exhibited a significant contribution to total resistance of the device. This finding confirms that the 2D interlayer effectively reduces the contact resistance bottleneck in WS_2 devices. It highlights how controlling interface states and energy band alignment at the contact can lead to significant performance gains. Importantly, this contact engineering concept can be applicable to other 2D-material devices. 2D interlayer schemes could improve contacts in photodetectors, LEDs, neuromorphic synapses, or biosensors - all of which suffer from Fermi-level pinning at the metal/2D interface[14]. In summary, the use of an ultrathin 2D interlayer at the source/drain contacts proved to be a viable and scalable strategy to enhance 2D device performance, yielding statistically significant gains in all key metrics. This study provided the first statistical validation that van der Waals interface engineering can systematically tune contact properties and consistently improve device performance across many devices, rather than just in single-device demonstrations.

The third major part of this work focused on gate-stack engineering for 2D FETs, addressing the longstanding challenge of integrating high-quality high-κ dielectrics on atomically flat semiconductors. This effort required recognizing that the chemically inert nature of pristine 2D surfaces prevents ALD precursors from forming continuous films in the absence of nucleation

sites. A novel approach was developed using metal TMDs as van der Waals seed layers to facilitate ALD of high-κ dielectrics. It was discovered that certain layered metal dichalcogenides (such as $TaSe_2$, $TaTe_2$, $NbSe_2$, $NbTe_2$, $PdSe_2$, and $PtSe_2$) can be exfoliated as monolayers and will spontaneously oxidize in ambient conditions, forming ultrathin, uniform metal-oxide films on the 2D semiconductor surface. These oxidized monolayers served as an ideal nucleation layers for subsequent ALD. Using this method, conformal HfO_2 films ~5 nm thick were deposited on MoS_2 and WSe_2 channels, achieving a much more uniform and reliable gate dielectric than direct ALD on pristine 2D surfaces. The electrical characterization of these seed-layer-integrated gate stacks showed reliable dielectric properties. For instance, the monolayer-seeded HfO_2 films sustained breakdown field strengths comparable to the best reported ALD oxides on 2D materials, while the leakage current at 1 V bias was kept below 10^{-2} A/cm^2 – satisfying the targets for high-performance logic devices. Remarkably, the vdW seed layers oxidize into high-κ oxides themselves, effectively becoming part of an ultrathin dielectric and further boosting the gate stack capacitance. To validate the device-level impact, dual-gate 2D FETs were implemented by combining the back-gate with the new top-gate stack. These bilayer WSe_2 (p-type) and monolayer MoS_2 (n-type) transistors with HfO_2 top dielectrics exhibited high on/off ratios (10^5–10^7) and steep subthreshold swings. Notably, n-type MoS_2 devices achieved subthreshold swings as low as 64 mV/dec at V_{DS} = 1 V – approaching the theoretical limit – even with a sub-300 nm gate length. Such steep slopes at short gate lengths reflect the excellent electrostatic control afforded by the high-quality, high-κ gate stack and the dual-gate configuration. Additionally, these devices showed minimal hysteresis (25 mV) in dual-sweep measurements, indicating low density of interface traps in the semiconductor/dielectric stack. What makes the seed-layer strategy particularly appealing is its dual character: at the bottom interface, the semiconductor remains coupled through van der Waals interactions that preserves its intrinsic properties, while at the top surface, spontaneous oxidation of the metallic monolayer generates nucleation sites that enable uniform ALD growth of high-κ dielectrics. This unique combination circumvents the long-standing dilemma of balancing interface cleanliness with dielectric processability, offering a chemically inert channel interface together with a chemically active dielectric interface. Altogether, these findings establish vdW seed layers as a powerful route to overcoming the dielectric integration bottleneck in 2D electronics, while also demonstrating their ability to enable robust and scalable device operation. It underscores that careful control of interface and seed layer formation is key to achieving high-quality, reliable gate dielectrics on 2D materials.

In summary, the key outcomes of this dissertation include:

1. **The development and understanding of a scalable exfoliation method** that enabled the preparation of complementary 2D semiconductors for FETs and circuits, while also shedding light on the physical limitations and opportunities associated with large-area monolayer integration.
2. **The exploration of contact resistance reduction through interlayer engineering,** which not only provided a viable strategy to lower R_c and enhance device performance, but also offered new insight into the mechanisms of charge injection and Fermi-level pinning at metal/semiconductor interfaces.
3. **The demonstration of van der Waals seed-layer-assisted gate dielectric integration,** achieving ultrathin high-κ stacks with robust electrical properties, and at the same time deepening the understanding of ALD nucleation processes on inert surface of 2D materials.

Importantly, these outcomes were achieved through in-depth exploration of the factors governing layer, contact, and dielectric quality. Beyond the technical advances themselves, these studies also provided valuable insights into the underlying challenges of contact resistance, dielectric nucleation, and interface control in 2D semiconductors. By systematically exploring these issues, the work contributes to a deeper understanding of the mechanisms that limit device behavior and outlines pathways for overcoming them. While the approaches developed here are best suited for research and prototyping environments, they nonetheless highlight the potential of careful interface and material engineering to enable more reliable and better-performing 2D devices.

7.2. Remaining challenges and future outlook

While substantial progress in the area of interface engineering and large-area integration has been made in this work, several open challenges and avenues for future research remain on the road to practical 2D CMOS technologies. Scalability is a foremost concern. The techniques demonstrated, particularly gold-assisted exfoliation and transfer of 2D layers, while effective at the sample scale, must be translated to true wafer-scale production. Currently, the highest-performing devices still rely on exfoliated materials or 1 cm x 1 cm MOCVD layers, but these approaches lack the throughput and uniformity required for mass production. Moving forward, efforts should focus on adapting exfoliation techniques into a more automated or continuous process – for example, roll-to-roll or wafer-level stamping of 2D monolayers. In parallel,

improvements in direct 2D material growth are crucial. CVD and MOCVD have shown promise for growing monolayer TMDs over large areas, but issues such as grain boundaries, thickness inhomogeneities, and defects currently limit device uniformity and yield. Future research should aim to reduce grain boundary densities and mosaic spread in CVD-grown films to approach the electronic quality of exfoliated flakes. The integration of n- and p-type 2D materials on a common substrate remains a central challenge for achieving scalable complementary logic. While demonstrations of such integration have already been reported[12,123], the approaches used to date often face limitations in terms of device yield, uniformity, and electrical performance. Further optimization of transfer-based strategies, for example, assembling pre-grown n- and p-type monolayers into a single heterogeneous wafer, could provide a practical near-term route. In the longer term, methods such as selective area growth of distinct TMDs on the same platform hold promise for advancing toward more seamless and monolithic 2D CMOS integration with improved device metrics.

Another persistent challenge is interface contamination and processing-induced disorder, which can undermine the advantages of the engineered approaches. In this work, polymer-supported transfer and gold tape (for both contact interlayers and channel placement) was employed, and while reasonably successful, it inevitably introduced residues and adsorbates on the 2D surfaces. Such contaminants can scatter carriers and pin charges, preventing devices from reaching their intrinsic limits. Future optimization will require cleaner transfer and assembly techniques – for instance, water- or thermal release tapes that leave less residue, transfers in inert environments, or completely adhesive-free van der Waals pick-and-place methods. Recent advances in growth of 2D heterostructures (growing one 2D material directly on another)[174,175] are particularly promising, as they can yield atomically clean interfaces without any polymer introduction. Extending such direct synthesis techniques to the MoS_2/WS_2 (or WSe_2) contact system explored here could eliminate the contamination at the interface and potentially push contact resistances toward record-low values. Similarly, for the gate stack, while the vdW seed layer ALD method is intrinsically better than plasma functionalization, controlling the interface cleanliness prior to seed placement will be vital. Any residual contaminants on the 2D channel before seed layer deposition could become trapped under the dielectric, so future work might integrate a gentle pre-clean (such as mild plasma treatments optimized to not damage the 2D layer) immediately before laying down the metal seed. Ensuring long-term device stability remains an important consideration, since 2D FETs are inherently sensitive to ambient exposure, which can induce oxidation, moisture uptake, and consequently threshold voltage

shifts or mobility degradation. In practice, this challenge is addressed by encapsulating the active channel. While exfoliated materials such as hBN have been frequently employed in research[176,177], they are not scalable for technological applications. In contrast, devices incorporating a top-gate dielectric grown by ALD inherently achieve encapsulation, as the conformal oxide layer covers both the channel and surrounding regions, effectively protecting the device from environmental degradation while simultaneously serving its gating function.

Device variability and yield are also critical concerns moving forward. Although the statistical approach in this dissertation established that the proposed methods consistently improve performance, the absolute spread in device parameters (e.g. threshold voltage or mobility distributions) in 2D devices is still broader than in silicon CMOS. Part of this variability stems from the aforementioned material non-uniformities; another part comes from device-scale factors like edge defects, contact placement accuracy, and unintentional doping from the environment. Future research should pursue strategies to tighten the distributions of key metrics. Moreover, statistical variability studies should be expanded to capture reliability metrics – for instance, variability in threshold shift under bias stress or hysteresis – to ensure that the engineered solutions hold under operating conditions expected in real circuits.

Several specific research directions emerge from the advances in this thesis. For the contact interlayer concept, investigating other material combinations would be worthwhile. The MoS_2-on-WS_2 system proved effective; one could explore, for example, whether an interlayer can also improve p-type contacts, since achieving high-performance p-type devices remains a challenge. Additionally, integrating the interlayer in a more seamless way is an open question – instead of a transfer, can one grow a monolayer selectively at the contact regions. Achieving an in situ grown monolayer interlayer would lead to improvement in contact resistances, as it would ensure an atomically clean, perfectly registered interface without manual assembly. Furthermore, combining the interlayer approach with doping techniques could yield even lower contact resistances. This remains challenging for 2D materials, but advances in doping may eventually allow spatially localized doping that complements the interlayer's effect. For the gate dielectric integration, future work might explore the limits of scaling and new materials. The demonstrated 5 nm HfO_2 films are already quite thin, but continued scaling of equivalent oxide thickness will be needed as transistors shrink.

In conclusion, the advances achieved in this dissertation – from resistance-reduced contacts to high-quality gate dielectrics and demonstration of complementary logic – represent significant

steps forward for 2D FET technology. Equally important, this work has provided a deeper understanding of the mechanisms that govern device behavior, including charge injection across interfaces, nucleation of dielectrics on inert surfaces, and electrostatic control in atomically thin channels. Such insights are essential, as progress in this field depends not only on demonstrating devices but also on revealing the underlying phenomena that limit or enable their performance. Yet, continued research and development are required to fully realize 2D materials in useful electronics. By addressing scalability, ensuring cleanliness, minimizing variability, and integrating with mainstream processes, the concepts presented here can be further optimized. The future outlook for 2D electronics is thus one of cautious optimism: the foundational pieces – high-mobility channels, ohmic contacts, robust high-κ gates, and complementary operation – are falling into place, and the next few years will likely see rapid progress in unifying these into practical, scalable 2D systems. Overcoming the remaining challenges will demand interdisciplinary efforts spanning materials science, physics, device engineering, and circuit design. If successful, the reward will be a new generation of electronic technology leveraging the atomic precision and novel properties of 2D materials – enabling ultra-scaled transistors, three-dimensional integrated circuits, and innovative systems that extend beyond the limits of conventional silicon CMOS. The work presented in this dissertation contributes to this broader effort by showing that careful interface engineering combined with physical insight can both improve device performance and clarify the principles that will guide the evolution of all-2D electronics.

List of references

1. Dickinson, R. G. & Pauling, L. THE CRYSTAL STRUCTURE OF MOLYBDENITE. *J. Am. Chem. Soc.* **45**, 1466–1471 (1923).
2. Seonghoon Jin, Fischetti, M. V., & Ting-Wei Tang. Modeling of Surface-Roughness Scattering in Ultrathin-Body SOI MOSFETs. *IEEE Trans. Electron Devices* **54**, 2191–2203 (2007).
3. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS2 transistors. *Nature Nanotech* **6**, 147–150 (2011).
4. Wang, Q. H., Kalantar-Zadeh, K., Kis, A., Coleman, J. N. & Strano, M. S. Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. *Nature Nanotech* **7**, 699–712 (2012).
5. Jariwala, D., Sangwan, V. K., Lauhon, L. J., Marks, T. J. & Hersam, M. C. Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides. *ACS Nano* **8**, 1102–1120 (2014).
6. Chen, J. *et al.* Performance Limits and Advancements in Single 2D Transition Metal Dichalcogenide Transistor. *Nano-Micro Lett.* **16**, 264 (2024).
7. Dorow, C. J. *et al.* Gate length scaling beyond Si: Mono-layer 2D Channel FETs Robust to Short Channel Effects. in *2022 International Electron Devices Meeting (IEDM)* 7.5.1-7.5.4 (IEEE, San Francisco, CA, USA, 2022). doi:10.1109/IEDM45625.2022.10019524.
8. Quellmalz, A. *et al.* Large-area integration of two-dimensional materials and their heterostructures by wafer bonding. *Nat Commun* **12**, 917 (2021).
9. Wang, S., Liu, X. & Zhou, P. The Road for 2D Semiconductors in the Silicon Age. *Advanced Materials* **34**, 2106886 (2022).
10. Kim, K. S. *et al.* The future of two-dimensional semiconductors beyond Moore's law. *Nat. Nanotechnol.* **19**, 895–906 (2024).

11. Huang, X., Liu, C. & Zhou, P. 2D semiconductors for specific electronic applications: from device to system. *npj 2D Mater Appl* **6**, 51 (2022).

12. Jayachandran, D. *et al.* Three-dimensional integration of two-dimensional field-effect transistors. *Nature* **625**, 276–281 (2024).

13. Contacts in 2D. *Nat Electron* **5**, 255–255 (2022).

14. Liu, X., Choi, M. S., Hwang, E., Yoo, W. J. & Sun, J. Fermi Level Pinning Dependent 2D Semiconductor Devices: Challenges and Prospects. *Advanced Materials* **34**, 2108425 (2022).

15. Pan, Y. *et al.* Precise p-type and n-type doping of two-dimensional semiconductors for monolithic integrated circuits. *Nat Commun* **15**, 9631 (2024).

16. McDonnell, S. *et al.* HfO_2 on MoS_2 by Atomic Layer Deposition: Adsorption Mechanisms and Thickness Scalability. *ACS Nano* **7**, 10354–10361 (2013).

17. Kim, Y. H. *et al.* Gate stack engineering of two-dimensional transistors. *Nat Electron* **8**, 770–783 (2025).

18. Knobloch, T. *et al.* Improving stability in two-dimensional transistors with amorphous gate oxides by Fermi-level tuning. *Nat Electron* **5**, 356–366 (2022).

19. Ly, T. H. *et al.* Misorientation-angle-dependent electrical transport across molybdenum disulfide grain boundaries. *Nat Commun* **7**, 10426 (2016).

20. Xia, Y. *et al.* 12-inch growth of uniform MoS2 monolayer for integrated circuit manufacture. *Nat. Mater.* **22**, 1324–1331 (2023).

21. Chamlagain, B. & Khondaker, S. I. Rapid Degradation of the Electrical Properties of 2D MoS_2 Thin Films under Long-Term Ambient Exposure. *ACS Omega* **6**, 24075–24081 (2021).

22. Qin, B. *et al.* General low-temperature growth of two-dimensional nanosheets from layered and nonlayered materials. *Nat Commun* **14**, 304 (2023).

23. Song, I., Park, C. & Choi, H. C. Synthesis and properties of molybdenum disulphide: from bulk to atomic layers. *RSC Adv.* **5**, 7495–7514 (2015).

24. Schulman, D. S., Arnold, A. J. & Das, S. Contact engineering for 2D materials and devices. *Chem. Soc. Rev.* **47**, 3037–3058 (2018).

25. Gusakova, J. *et al.* Electronic Properties of Bulk and Monolayer TMDs: Theoretical Study Within DFT Framework (GVJ-2e Method). *Physica Status Solidi (a)* **214**, 1700218 (2017).

26. Liu, G.-B., Shan, W.-Y., Yao, Y., Yao, W. & Xiao, D. Three-band tight-binding model for monolayers of group-VIB transition metal dichalcogenides. *Phys. Rev. B* **88**, 085433 (2013).

27. Kormányos, A. *et al.* **k** · **p** theory for two-dimensional transition metal dichalcogenide semiconductors. *2D Mater.* **2**, 022001 (2015).

28. Rasmussen, F. A. & Thygesen, K. S. Computational 2D Materials Database: Electronic Structure of Transition-Metal Dichalcogenides and Oxides. *J. Phys. Chem. C* **119**, 13169–13183 (2015).

29. Vurgaftman, I., Meyer, J. R. & Ram-Mohan, L. R. Band parameters for III–V compound semiconductors and their alloys. *Journal of Applied Physics* **89**, 5815–5875 (2001).

30. Thomas, N. *et al.* 2D MoS2: structure, mechanisms, and photocatalytic applications. *Materials Today Sustainability* **13**, 100073 (2021).

31. Lopez-Sanchez, O., Lembke, D., Kayci, M., Radenovic, A. & Kis, A. Ultrasensitive photodetectors based on monolayer MoS2. *Nature Nanotech* **8**, 497–501 (2013).

32. Mak, K. F., Lee, C., Hone, J., Shan, J. & Heinz, T. F. Atomically Thin MoS 2 : A New Direct-Gap Semiconductor. *Phys. Rev. Lett.* **105**, 136805 (2010).

33. Li, H.-M. *et al.* Metal-Semiconductor Barrier Modulation for High Photoresponse in Transition Metal Dichalcogenide Field Effect Transistors. *Sci Rep* **4**, 4041 (2014).

34. Kim, C. *et al.* Fermi Level Pinning at Electrical Metal Contacts of Monolayer Molybdenum Dichalcogenides. *ACS Nano* **11**, 1588–1596 (2017).

35. Das, S., Chen, H.-Y., Penumatcha, A. V. & Appenzeller, J. High Performance Multilayer MoS_2 Transistors with Scandium Contacts. *Nano Lett.* **13**, 100–105 (2013).

36. Chen, R.-S., Ding, G., Zhou, Y. & Han, S.-T. Fermi-level depinning of 2D transition metal dichalcogenide transistors. *J. Mater. Chem. C* **9**, 11407–11427 (2021).

37. Chuang, S. *et al.* MoS_2 P-type Transistors and Diodes Enabled by High Work Function MoO_x Contacts. *Nano Lett.* **14**, 1337–1342 (2014).

38. Wang, W. *et al.* Controllable Schottky Barriers between MoS2 and Permalloy. *Sci Rep* **4**, 6928 (2014).

39. Cho, K. *et al.* Contact-Engineered Electrical Properties of MoS_2 Field-Effect Transistors via Selectively Deposited Thiol-Molecules. *Advanced Materials* **30**, 1705540 (2018).

40. Chanana, A. & Mahapatra, S. Prospects of zero Schottky barrier height in a graphene-inserted MoS2-metal interface. *Journal of Applied Physics* **119**, 014303 (2016).

41. Farmanbar, M. & Brocks, G. Ohmic Contacts to 2D Semiconductors through van der Waals Bonding. *Adv Elect Materials* **2**, 1500405 (2016).

42. Liu, Y., Xiao, H. & Goddard, W. A. Schottky-Barrier-Free Contacts with Two-Dimensional Semiconductors by Surface-Engineered MXenes. *J. Am. Chem. Soc.* **138**, 15853–15856 (2016).

43. Telford, E. J. *et al.* Via Method for Lithography Free Contact and Preservation of 2D Materials. *Nano Lett.* **18**, 1416–1420 (2018).

44. Jang, J. *et al.* Fermi-Level Pinning-Free WSe_2 Transistors via 2D Van der Waals Metal Contacts and Their Circuits. *Advanced Materials* **34**, 2109899 (2022).

45. Liu, Y., Stradins, P. & Wei, S.-H. Van der Waals metal-semiconductor junction: Weak Fermi level pinning enables effective tuning of Schottky barrier. *Sci. Adv.* **2**, e1600069 (2016).

46. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High Current Density in Monolayer MoS_2 Doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).

47. Kiriya, D., Tosun, M., Zhao, P., Kang, J. S. & Javey, A. Air-Stable Surface Charge Transfer Doping of MoS_2 by Benzyl Viologen. *J. Am. Chem. Soc.* **136**, 7853–7856 (2014).

48. Lan, H.-Y. *et al.* Uncovering the doping mechanism of nitric oxide in high-performance P-type WSe2 transistors. *Nat Commun* **16**, 4160 (2025).

49. Parto, K. *et al.* One-Dimensional Edge Contacts to Two-Dimensional Transition-Metal Dichalcogenides: Uncovering the Role of Schottky-Barrier Anisotropy in Charge Transport across Mo S 2 /Metal Interfaces. *Phys. Rev. Applied* **15**, 064068 (2021).

50. Zheng, Y., Gao, J., Han, C. & Chen, W. Ohmic Contact Engineering for Two-Dimensional Materials. *Cell Reports Physical Science* **2**, 100298 (2021).

51. Cheng, Z. *et al.* Immunity to Contact Scaling in MoS_2 Transistors Using in Situ Edge Contacts. *Nano Lett.* **19**, 5077–5085 (2019).

52. Shetty, N. *et al.* Scalable Fabrication of Edge Contacts to 2D Materials: Implications for Quantum Resistance Metrology and 2D Electronics. *ACS Appl. Nano Mater.* **6**, 6292–6298 (2023).

53. Lin, C.-C. *et al.* Interfacial Elemental Analysis of Slanted Edge-Contacted Monolayer MoS_2 Transistors via Directionally Angled Etching. *ACS Nano* **19**, 4452–4461 (2025).

54. Shen, P.-C. *et al.* Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).

55. Li, W. *et al.* Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **613**, 274–279 (2023).

56. Yang, S. *et al.* Gate Dielectrics Integration for 2D Electronics: Challenges, Advances, and Outlook. *Advanced Materials* **35**, 2207901 (2023).

57. Schilirò, E., Lo Nigro, R., Roccaforte, F. & Giannazzo, F. Substrate-Driven Atomic Layer Deposition of High-κ Dielectrics on 2D Materials. *Applied Sciences* **11**, 11052 (2021).

58. Cheng, L. *et al.* Atomic Layer Deposition of a High- *k* Dielectric on MoS_2 Using Trimethylaluminum and Ozone. *ACS Appl. Mater. Interfaces* **6**, 11834–11838 (2014).

59. Azcatl, A. *et al.* HfO_2 on UV–O_3 exposed transition metal dichalcogenides: interfacial reactions study. *2D Mater.* **2**, 014004 (2015).

60. Park, J. H. *et al.* Atomic Layer Deposition of Al_2O_3 on WSe_2 Functionalized by Titanyl Phthalocyanine. *ACS Nano* **10**, 6888–6896 (2016).

61. Ko, J.-S. *et al.* Sub-Nanometer Equivalent Oxide Thickness and Threshold Voltage Control Enabled by Silicon Seed Layer on Monolayer MoS_2 Transistors. *Nano Lett.* **25**, 2587–2593 (2025).

62. McDonnell, S. J. & Wallace, R. M. Atomically-thin layered films for device applications based upon 2D TMDC materials. *Thin Solid Films* **616**, 482–501 (2016).

63. Li, T. *et al.* A native oxide high-κ gate dielectric for two-dimensional electronics. *Nat Electron* **3**, 473–478 (2020).

64. Hou, X., Jin, T., Zheng, Y. & Chen, W. Atomic-scale interface engineering for two-dimensional materials based field-effect transistors. *SmartMat* **5**, e1236 (2024).

65. Chen, J. *et al.* Vertically grown ultrathin Bi2SiO5 as high-κ single-crystalline gate dielectric. *Nat Commun* **14**, 4406 (2023).

66. Liu, K. *et al.* A wafer-scale van der Waals dielectric made from an inorganic molecular crystal film. *Nat Electron* **4**, 906–913 (2021).

67. Vu, Q. A. *et al.* Near-zero hysteresis and near-ideal subthreshold swing in h-BN encapsulated single-layer MoS_2 field-effect transistors. *2D Mater.* **5**, 031001 (2018).

68. Kropp, J. A., Sharma, A., Zhu, W., Ataca, C. & Gougousi, T. Surface Defect Engineering of MoS_2 for Atomic Layer Deposition of TiO_2 Films. *ACS Appl. Mater. Interfaces* **12**, 48150–48160 (2020).

69. Price, K. M., Schauble, K. E., McGuire, F. A., Farmer, D. B. & Franklin, A. D. Uniform Growth of Sub-5-Nanometer High-κ Dielectrics on MoS_2 Using Plasma-Enhanced Atomic Layer Deposition. *ACS Appl. Mater. Interfaces* **9**, 23072–23080 (2017).

70. Price, K. M. *et al.* Plasma-Enhanced Atomic Layer Deposition of HfO_2 on Monolayer, Bilayer, and Trilayer MoS_2 for the Integration of High-κ Dielectrics in Two-Dimensional Devices. *ACS Appl. Nano Mater.* **2**, 4085–4094 (2019).

71. Li, W. *et al.* Uniform and ultrathin high-κ gate dielectrics for two-dimensional electronic devices. *Nat Electron* **2**, 563–571 (2019).

72. Zou, X. *et al.* Interface Engineering for High-Performance Top-Gated MoS_2 Field-Effect Transistors. *Advanced Materials* **26**, 6255–6261 (2014).

73. Dahal, A. *et al.* Seeding Atomic Layer Deposition of Alumina on Graphene with Yttria. *ACS Appl. Mater. Interfaces* **7**, 2082–2087 (2015).

74. Cassabois, G., Valvin, P. & Gil, B. Hexagonal boron nitride is an indirect bandgap semiconductor. *Nature Photon* **10**, 262–266 (2016).

75. Wang, L. *et al.* One-Dimensional Electrical Contact to a Two-Dimensional Material. *Science* **342**, 614–617 (2013).

76. Hui, F. *et al.* On the use of two dimensional hexagonal boron nitride as dielectric. *Microelectronic Engineering* **163**, 119–133 (2016).

77. Söll, A. *et al.* High-κ Wide-Gap Layered Dielectric for Two-Dimensional van der Waals Heterostructures. *ACS Nano* **18**, 10397–10406 (2024).

78. Xu, F. *et al.* Few-Layered $MnAl_2S_4$ Dielectrics for High-Performance van der Waals Stacked Transistors. *ACS Appl. Mater. Interfaces* **14**, 25920–25927 (2022).

79. Huang, J.-K. *et al.* High-κ perovskite membranes as insulators for two-dimensional transistors. *Nature* **605**, 262–267 (2022).

80. Mleczko, M. J. *et al.* $HfSe_2$ and $ZrSe_2$: Two-dimensional semiconductors with native high-κ oxides. *Sci. Adv.* **3**, e1700481 (2017).

81. Islam, M. A. *et al.* Exfoliation mechanisms of 2D materials and their applications. *Applied Physics Reviews* **9**, 041301 (2022).

82. Li, Y., Kuang, G., Jiao, Z., Yao, L. & Duan, R. Recent progress on the mechanical exfoliation of 2D transition metal dichalcogenides. *Mater. Res. Express* **9**, 122001 (2022).

83. Kang, K. *et al.* High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature* **520**, 656–660 (2015).

84. Eichfeld, S. M. *et al.* Highly Scalable, Atomically Thin WSe_2 Grown *via* Metal–Organic Chemical Vapor Deposition. *ACS Nano* **9**, 2080–2087 (2015).

85. Coleman, J. N. *et al.* Two-Dimensional Nanosheets Produced by Liquid Exfoliation of Layered Materials. *Science* **331**, 568–571 (2011).

86. Nicolosi, V., Chhowalla, M., Kanatzidis, M. G., Strano, M. S. & Coleman, J. N. Liquid Exfoliation of Layered Materials. *Science* **340**, 1226419 (2013).

87. Jiao, L. *et al.* Molecular-beam epitaxy of monolayer $MoSe_2$: growth characteristics and domain boundary formation. *New J. Phys.* **17**, 053023 (2015).

88. Huang, Y. *et al.* Universal mechanical exfoliation of large-area 2D crystals. *Nat Commun* **11**, 2453 (2020).

89. Velický, M. *et al.* Mechanism of Gold-Assisted Exfoliation of Centimeter-Sized Transition-Metal Dichalcogenide Monolayers. *ACS Nano* **12**, 10463–10472 (2018).

90. Momeni, K. *et al.* A computational framework for guiding the MOCVD-growth of wafer-scale 2D materials. *npj Comput Mater* **8**, 240 (2022).

91. Lee, D. H., Sim, Y., Wang, J. & Kwon, S.-Y. Metal–organic chemical vapor deposition of 2D van der Waals materials—The challenges and the extensive future opportunities. *APL Materials* **8**, 030901 (2020).

92. Heyl, M. & List-Kratochvil, E. J. W. Only gold can pull this off: mechanical exfoliations of transition metal dichalcogenides beyond scotch tape. *Appl. Phys. A* **129**, 16 (2023).

93. Wang, Z. & Zhang, Z. Electron Beam Evaporation Deposition. in *Advanced Nano Deposition Methods* (eds. Lin, Y. & Chen, X.) 33–58 (Wiley, 2016). doi:10.1002/9783527696406.ch2.

94. Shen, X., Wang, H. & Yu, T. How do the electron beam writing and metal deposition affect the properties of graphene during device fabrication? *Nanoscale* **5**, 3352 (2013).

95. Das, S. *et al.* Transistors based on two-dimensional materials for future integrated circuits. *Nat Electron* **4**, 786–799 (2021).

96. Xiao, S. *et al.* Atomic-layer soft plasma etching of MoS2. *Sci Rep* **6**, 19945 (2016).

97. Chee, S. & Ham, M. Low-Damaged Layer-by-Layer Etching of Large-Area Molybdenum Disulfide Films via Mild Plasma Treatment. *Adv Materials Inter* **7**, 2000762 (2020).

98. Kim, M. *et al.* HfO2 etching mechanism in inductively-coupled Cl2/Ar plasma. *Thin Solid Films* **519**, 6708–6711 (2011).

99. Kim, D.-P. *et al.* Etching Properties of HfO_2 Thin Films in Cl_2 /BCl_3 /Ar Plasma. *Ferroelectrics* **381**, 30–40 (2009).

100. Mitta, S. B. *et al.* Electrical characterization of 2D materials-based field-effect transistors. *2D Mater.* **8**, 012002 (2021).

101. Ahmed, F., Choi, M. S., Liu, X. & Yoo, W. J. Carrier transport at the metal–MoS_2 interface. *Nanoscale* **7**, 9222–9228 (2015).

102. Paghi, A., Battisti, S., Tortorella, S., De Simoni, G. & Giazotto, F. Cryogenic behavior of high-permittivity gate dielectrics: The impact of atomic layer deposition temperature and the lithographic patterning method. *Journal of Applied Physics* **137**, 044103 (2025).

103. Zhang, L., Dong, J. & Ding, F. Strategies, Status, and Challenges in Wafer Scale Single Crystalline Two-Dimensional Materials Synthesis. *Chem. Rev.* **121**, 6321–6372 (2021).

104. Xue, G. *et al.* Large-Area Epitaxial Growth of Transition Metal Dichalcogenides. *Chem. Rev.* **124**, 9785–9865 (2024).

105. Sebastian, A., Pendurthi, R., Choudhury, T. H., Redwing, J. M. & Das, S. Benchmarking monolayer MoS2 and WS2 field-effect transistors. *Nat Commun* **12**, 693 (2021).

106. Eichfeld, S. M., Colon, V. O., Nie, Y., Cho, K. & Robinson, J. A. Controlling nucleation of monolayer WSe_2 during metal-organic chemical vapor deposition growth. *2D Mater.* **3**, 025015 (2016).

107. Liu, H. F., Wong, S. L. & Chi, D. Z. CVD Growth of MoS_2 -based Two-dimensional Materials. *Chemical Vapor Deposition* **21**, 241–259 (2015).

108. Panasci, S. E. *et al.* Strain, Doping, and Electronic Transport of Large Area Monolayer MoS_2 Exfoliated on Gold and Transferred to an Insulating Substrate. *ACS Appl. Mater. Interfaces* **13**, 31248–31259 (2021).

109. Giza, M. *et al.* Contact Resistance Engineering in WS_2 -Based FET with MoS_2 Under-Contact Interlayer: A Statistical Approach. *ACS Appl. Mater. Interfaces* **16**, 48556–48564 (2024).

110. Liu, F. *et al.* Disassembling 2D van der Waals crystals into macroscopic monolayers and reassembling into artificial lattices. *Science* **367**, 903–906 (2020).

111. Pan, Y. & Zahn, D. R. T. Raman Fingerprint of Interlayer Coupling in 2D TMDCs. *Nanomaterials* **12**, 3949 (2022).

112. Tonndorf, P. *et al.* Photoluminescence emission and Raman response of monolayer MoS_2, MoSe_2, and WSe_2. *Opt. Express* **21**, 4908 (2013).

113. McCreary, K. M., Hanbicki, A. T., Sivaram, S. V. & Jonker, B. T. A- and B-exciton photoluminescence intensity ratio as a measure of sample quality for transition metal dichalcogenide monolayers. *APL Materials* **6**, 111106 (2018).

114. Lee, C. *et al.* Anomalous Lattice Vibrations of Single- and Few-Layer MoS_2. *ACS Nano* **4**, 2695–2700 (2010).

115. Zhan, Y., Liu, Z., Najmaei, S., Ajayan, P. M. & Lou, J. Large Area Vapor Phase Growth and Characterization of MoS2 Atomic Layers on SiO2 Substrate.

116. Panasci, S. E., Schilirò, E., Roccaforte, F. & Giannazzo, F. Gold-Assisted Exfoliation of Large-Area Monolayer Transition Metal Dichalcogenides: From Interface Properties to Device Applications. *Adv Funct Materials* 2414532 (2024) doi:10.1002/adfm.202414532.

117. Fang, H. *et al.* High-Performance Single Layered WSe_2 p-FETs with Chemically Doped Contacts. *Nano Lett.* **12**, 3788–3792 (2012).

118. Cai, L. *et al.* Rapid Flame Synthesis of Atomically Thin MoO_3 down to Monolayer Thickness for Effective Hole Doping of WSe_2. *Nano Lett.* **17**, 3854–3861 (2017).

119. Chiang, C.-C., Lan, H.-Y., Pang, C.-S., Appenzeller, J. & Chen, Z. Air-Stable P-Doping in Record High-Performance Monolayer WSe_2 Devices. *IEEE Electron Device Lett.* **43**, 319–322 (2022).

120. Vu, V. T. *et al.* One-Step Synthesis of $NbSe_2$ /Nb-Doped-WSe_2 Metal/Doped-Semiconductor van der Waals Heterostructures for Doping Controlled Ohmic Contact. *ACS Nano* **15**, 13031–13040 (2021).

121. Yang, S., Lee, G. & Kim, J. Selective p-Doping of 2D WSe_2 *via* UV/Ozone Treatments and Its Application in Field-Effect Transistors. *ACS Appl. Mater. Interfaces* **13**, 955–961 (2021).

122. Pandey, S. K. *et al.* Controlled p-type substitutional doping in large-area monolayer WSe_2 crystals grown by chemical vapor deposition. *Nanoscale* **10**, 21374–21385 (2018).

123. Pendurthi, R. *et al.* Monolithic three-dimensional integration of complementary two-dimensional field-effect transistors. *Nat. Nanotechnol.* **19**, 970–977 (2024).

124. Lan, H.-Y., Tripathi, R., Liu, X., Appenzeller, J. & Chen, Z. Wafer-scale CVD Monolayer WSe_2 p-FETs with Record-high 727 μA/μm I_{on} and 490 μS/ μm g_{max} via Hybrid Charge Transfer and Molecular Doping. in *2023 International Electron Devices Meeting (IEDM)* 1–4 (IEEE, San Francisco, CA, USA, 2023). doi:10.1109/IEDM45741.2023.10413736.

125. Dorow, C. J. *et al.* Exploring manufacturability of novel 2D channel materials: 300 mm wafer-scale 2D NMOS & PMOS using MoS_2 , WS_2 , & WSe_2. in *2023 International Electron Devices Meeting (IEDM)* 1–4 (IEEE, San Francisco, CA, USA, 2023). doi:10.1109/IEDM45741.2023.10413874.

126. Mortelmans, W. *et al.* Record Performance in GAA 2D NMOS and PMOS Using Monolayer MoS2 and WSe2 with Scaled Contact and Gate Length. in *2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* 1–2 (IEEE, Honolulu, HI, USA, 2024). doi:10.1109/VLSITechnologyandCir46783.2024.10631395.

127. Oberoi, A. *et al.* Toward High-Performance p-Type Two-Dimensional Field Effect Transistors: Contact Engineering, Scaling, and Doping. *ACS Nano* **17**, 19709–19723 (2023).

128. Patoary, N. H. *et al.* Improvements in 2D p-type WSe2 transistors towards ultimate CMOS scaling. *Sci Rep* **13**, 3304 (2023).

129. Liu, X. *et al.* High performance WSe2 p-MOSFET with intrinsic n-channel based on back-to-back p–n junctions. *Applied Physics Letters* **118**, 233101 (2021).

130. Kwon, J. *et al.* 200-mm-wafer-scale integration of polycrystalline molybdenum disulfide transistors. *Nat Electron* **7**, 356–364 (2024).

131. Chou, A.-S. *et al.* Antimony Semimetal Contact with Enhanced Thermal Stability for High Performance 2D Electronics. in *2021 IEEE International Electron Devices Meeting (IEDM)* 7.2.1-7.2.4 (IEEE, San Francisco, CA, USA, 2021). doi:10.1109/IEDM19574.2021.9720608.

132. Chou, A.-S. *et al.* High On-Current 2D nFET of 390 μA/μm at VDS = 1V using Monolayer CVD MoS2 without Intentional Doping. in *2020 IEEE Symposium on VLSI Technology* 1–2 (IEEE, Honolulu, HI, USA, 2020). doi:10.1109/VLSITechnology18217.2020.9265040.

133. Sik Hwang, W. *et al.* Comparative study of chemically synthesized and exfoliated multilayer MoS2 field-effect transistors. *Applied Physics Letters* **102**, 043116 (2013).

134. English, C. D., Shine, G., Dorgan, V. E., Saraswat, K. C. & Pop, E. Improved Contacts to MoS $_2$ Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett.* **16**, 3824–3830 (2016).

135. Wachter, S., Polyushkin, D. K., Bethge, O. & Mueller, T. A microprocessor based on a two-dimensional semiconductor. *Nat Commun* **8**, 14948 (2017).

136. Shulaker, M. M. *et al.* Carbon nanotube computer. *Nature* **501**, 526–530 (2013).

137. Hills, G. *et al.* Modern microprocessor built from complementary carbon nanotube transistors. *Nature* **572**, 595–602 (2019).

138. Sarkar, D. *et al.* MoS_2 Field-Effect Transistor for Next-Generation Label-Free Biosensors. *ACS Nano* **8**, 3992–4003 (2014).

139. Chhowalla, M. *et al.* The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets. *Nature Chem* **5**, 263–275 (2013).

140. Haensch, W. *et al.* Silicon CMOS devices beyond scaling. *IBM J. Res. & Dev.* **50**, 339–361 (2006).

141. Kim, B.-K. *et al.* Origins of genuine Ohmic van der Waals contact between indium and MoS2. *npj 2D Mater Appl* **5**, 9 (2021).

142. Liu, L. *et al.* Transferred van der Waals metal electrodes for sub-1-nm MoS2 vertical transistors. *Nat Electron* **4**, 342–347 (2021).

143. Yang, L. *et al.* Chloride Molecular Doping Technique on 2D Materials: WS_2 and MoS_2. *Nano Lett.* **14**, 6275–6280 (2014).

144. Zhang, S. *et al.* Control of the Schottky barrier height in monolayer WS2 FETs using molecular doping. *AIP Advances* **12**, 085222 (2022).

145. Phan, N. A. N. *et al.* Enhanced Performance of WS_2 Field-Effect Transistor through Mono and Bilayer h-BN Tunneling Contacts. *Small* **18**, 2105753 (2022).

146. Wang, J. *et al.* High Mobility MoS_2 Transistor with Low Schottky Barrier Contact by Using Atomic Thick h-BN as a Tunneling Layer. *Advanced Materials* **28**, 8302–8308 (2016).

147. Andrews, K., Bowman, A., Rijal, U., Chen, P.-Y. & Zhou, Z. Improved Contacts and Device Performance in MoS_2 Transistors Using a 2D Semiconductor Interlayer. *ACS Nano* **14**, 6232–6241 (2020).

148. Tang, H. *et al.* Schottky Contact in Monolayer WS_2 Field-Effect Transistors. *Advcd Theory and Sims* **2**, 1900001 (2019).

149. Wang, Q., Shao, Y., Gong, P. & Shi, X. Metal–2D multilayered semiconductor junctions: layer-number dependent Fermi-level pinning. *J. Mater. Chem. C* **8**, 3113–3119 (2020).

150. Saito, Y. *et al.* Low frequency Raman study of interlayer couplings in WS_2–MoS_2 van der Waals heterostructures. *Jpn. J. Appl. Phys.* **59**, 062004 (2020).

151. Li, H. *et al.* From Bulk to Monolayer MoS_2 : Evolution of Raman Scattering. *Adv Funct Materials* **22**, 1385–1390 (2012).

152. McCreary, K. M. *et al.* The Effect of Preparation Conditions on Raman and Photoluminescence of Monolayer WS2. *Sci Rep* **6**, 35154 (2016).

153. Steinhoff, A. *et al.* Efficient Excitonic Photoluminescence in Direct and Indirect Band Gap Monolayer MoS $_2$. *Nano Lett.* **15**, 6841–6847 (2015).

154. Sitek, J. *et al.* Selective Growth of van der Waals Heterostructures Enabled by Electron-Beam Irradiation. *ACS Appl. Mater. Interfaces* **15**, 33838–33847 (2023).

155. Lin, D. *et al.* Dual gate synthetic WS_2 MOSFETs with 120μS/μm Gm 2.7μF/cm^2 capacitance and ambipolar channel. in *2020 IEEE International Electron Devices Meeting (IEDM)* 3.6.1-3.6.4 (IEEE, San Francisco, CA, USA, 2020). doi:10.1109/IEDM13553.2020.9372055.

156. Illarionov, Y. Yu. *et al.* Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors. *Nat Electron* **2**, 230–235 (2019).

157. Cui, X. *et al.* Multi-terminal transport measurements of MoS2 using a van der Waals heterostructure device platform. *Nature Nanotech* **10**, 534–540 (2015).

158. Holler, B. A., Crowley, K., Berger, M. & Gao, X. P. A. 2D Semiconductor Transistors with Van der Waals Oxide MoO_3 as Integrated High-κ Gate Dielectric. *Adv Elect Materials* **6**, 2000635 (2020).

159. Kim, B. S. Y. *et al.* Advances and Applications of Oxidized van der Waals Transition Metal Dichalcogenides. *Advanced Science* **11**, 2407175 (2024).

160. Hajiyev, P., Cong, C., Qiu, C. & Yu, T. Contrast and Raman spectroscopy study of single- and few-layered charge density wave material: 2H-TaSe2. *Sci Rep* **3**, 2593 (2013).

161. Barajas-Aguilar, A. H. *et al.* Crystalline structure, electronic and lattice-dynamics properties of NbTe2. *Sci Rep* **8**, 16984 (2018).

162. Buchkov, K. *et al.* Synthesis and characterization of 2D platinum diselenide. *J. Phys.: Conf. Ser.* **1492**, 012022 (2020).

163. Abdul-Aziz, O. *et al.* Resonance-induced anomalies in temperature-dependent Raman scattering of $PdSe_2$. *J. Mater. Chem. C* **12**, 11402–11411 (2024).

164. Gao, J. J. *et al.* Origin of the structural phase transition in single-crystal TaT e 2. *Phys. Rev. B* **98**, 224104 (2018).

165. Orchin, G. J. *et al.* Niobium diselenide superconducting photodetectors. *Applied Physics Letters* **114**, 251103 (2019).

166. Stathis, J. H. Reliability limits for the gate insulator in CMOS technology. *IBM J. Res. & Dev.* **46**, 265–286 (2002).

167. Robertson, J. High dielectric constant oxides. *Eur. Phys. J. Appl. Phys.* **28**, 265–291 (2004).

168. Lin, G. *et al.* Performance enhancement of monolayer MoS_2 transistors by atomic layer deposition of high- *k* dielectric assisted by Al_2 O_3 seed layer. *J. Phys. D: Appl. Phys.* **53**, 105103 (2020).

169. Xu, Y. *et al.* Scalable integration of hybrid high-κ dielectric materials on two-dimensional semiconductors. *Nat. Mater.* **22**, 1078–1084 (2023).

170. Liu, C. *et al.* Silicon/2D-material photodetectors: from near-infrared to mid-infrared. *Light Sci Appl* **10**, 123 (2021).

171. Wu, S. *et al.* Polarization photodetectors with configurable polarity transition enabled by programmable ferroelectric-doping patterns. *Nat Commun* **15**, 8743 (2024).

172. Wu, L. Ultrathin waveguides for 2D photonic integrated circuits. *Nat Rev Phys* **5**, 634–634 (2023).

173. Karbalaei Akbari, M. *et al.* Functional Two-Dimensional Materials for Bioelectronic Neural Interfacing. *JFB* **14**, 35 (2023).

174. Chakraborty, S. K., Kundu, B., Nayak, B., Dash, S. P. & Sahoo, P. K. Challenges and opportunities in 2D heterostructures for electronic and optoelectronic devices. *iScience* **25**, 103942 (2022).

175. Chen, Z. *et al.* Comparative coherence between layered and traditional semiconductors: unique opportunities for heterogeneous integration. *Int. J. Extrem. Manuf.* **5**, 042001 (2023).

176. Han, X., Lin, J., Liu, J., Wang, N. & Pan, D. Effects of Hexagonal Boron Nitride Encapsulation on the Electronic Structure of Few-Layer MoS_2. *J. Phys. Chem. C* **123**, 14797–14802 (2019).

177. Kim, Y. D. *et al.* Ultrafast Graphene Light Emitters. *Nano Lett.* **18**, 934–940 (2018).

List of publications, dissemination, awards, and projects

Author metrics

The author of this thesis has contributed to 4 scientific articles published in the international scientific literature. According to Google Scholar (Scopus), her h-index is 2 (2), and she was cited 27 times (24 times).

Publications

Directly related to the thesis

M. Giza, K. Mukhopadhyay, H. Ravichandran, A. Pannone, S. Ghosh, S. Das, ***"Exploring the Application of Gold-Assisted Exfoliation in Large-scale Integration of n-Type and p-Type 2D-FETs"***. Small Methods 2025, 2500559. DOI: 10.1002/smtd.202500559 (Impact factor **9.1**)

M. Giza, M. Świniarski, A. P. Gertych, K. Czerniak-Łosiewicz, M. Rogala, P. J. Kowalczyk, M. Zdrojek, **"*Contact Resistance Engineering in WS_2-Based FET with MoS_2 Under-Contact Interlayer: A Statistical Approach",*** ACS Applied Materials & Interfaces 2024 16 (36), 48556-48564, DOI: 10.1021/acsami.4c09688 (Impact factor **8.3**).

M. Giza, K. Mukhopadhyay, P. Venkatram, Z. Chen, S. Ghosh, C. Chen, R. Sanikop, B. Hengstebeck, D. Lei, Y. Yang, J. M. Redwing, I. Plutnarová, J. Luxa, Z. Sofer, S. Das, **"*Integration of high-κ gate dielectrics with 2D semiconductors via self-oxidizing vdW metal seed layers"*** (submitted).

Other publications

J. Sitek, K. Czerniak-Łosiewicz, A. P. Gertych, **M. Giza**, P. Dąbrowski, M. Rogala, K. Wilczyński, A. Kaleta, S. Kret, B. R. Conran, X. Wang, C. McAleese, M. Macha, A. Radenović, M. Zdrojek, I. Pasternak, W. Strupiński, **"*Selective Growth of van der Waals Heterostructures Enabled by Electron-Beam Irradiation",*** ACS Applied Materials & Interfaces 2023 15 (28), 33838-33847**,** DOI: 10.1021/acsami.3c02892 (Impact factor **9.5**).

K. Czerniak-Łosiewicz, M. Świniarski, A. P. Gertych, **M. Giza**, Z. Maj, M. Rogala, P. J. Kowalczyk, M. Zdrojek, **"*Unraveling the Mechanism of the 150-Fold Photocurrent Enhancement in Plasma-Treated 2D TMDs",*** ACS Applied Materials & Interfaces 2022 14 (29), 33984-33992**,** DOI: 10.1021/acsami.2c06578 (Impact factor **10.3**).

Dissemination

Poster presentations

"Integration of high-κ gate dielectrics with 2D semiconductors via self-oxidizing vdW metal seed layers", Nature Low-Dimensional Electronics Conference, Beijing, China, 2025.

"Van der Waals seed layer strategy for reliable high-κ dielectric integration on 2D semiconductors", Flatlands Beyond Graphene Conference, Milan, Italy, 2025.

"Contact resistance engineering in WS_2-based FET with MoS_2 under-contact interlayer – statistical approach", Graphene 2024 Conference, Madrid, Spain, 2024.

"Electrical characterization of field-effect transistors based on monolayer WS_2 fabricated with gold-assisted exfoliation", Graphene and Other 2D Materials Conference, Toruń, Poland, 2023.

"Performance analysis of field-effect transistors based on monolayer WS_2 fabricated with gold-assisted exfoliation", Graphene 2023 Conference, Manchester, United Kingdom, 2023.

Oral presentations

"Influence of 2-dimensional interlayers on contact resistance in TMDs-based field-effect transistors", Conference Graphene and other 2D Materials, Łódź, Poland, 2022.

„Produkcja i characteryzacja nanourządzeń opartych na nowych materiałach monowarstwowych", Seminar of Research Centers for Priority Research Areas - Materials Technologies, online, 2022.

Patents

Patent Application (P.448796): *„Sposób wytwarzania heterostruktury złożonej z co najmniej dwóch monowarstw materiałów dwuwymiarowych o kontrolowanych kształtach"*, submitted.

Awards

Individual awards

Poster Award, Nature Low-Dimensional Electronics Conference, Peking University, Beijing, China, September 18–19, 2025, for the poster ***"Integration of high-κ gate dielectrics with 2D semiconductors via self-oxidizing vdW metal seed layers."***

Group awards

Rector's of WUT Scientific Team Award of first degree 2023

Projects

As a contractor

Stipendist, NCN Preludium Bis 2: *Novel van der Waals heterostructures for next-generation nano- and optoelectronics* (2020/39/O/ST5/00416), 2021–2025.

Contractor, WUT Grant in Physical Sciences: *Raman temperature studies of 2D materials and their heterostructures in vacuum*, 2022.

Contractor, POB-TM2 Start: *Production and characterization of nanodevices based on novel monolayer materials*, 2021–2022.

Foreign visits

Research Intern, Penn State University, USA (Das Research Group), 2024–2025 – Six-month research internship funded by NAWA within the NCN *Preludium Bis 2* project (*Novel van der Waals heterostructures for next-generation nano- and optoelectronics*), focused on fabrication and characterization of 2D devices using gold-assisted exfoliation.

Visiting Scholar, Penn State University, USA (Das Research Group), 2025 – Five-month extended stay funded by Penn State University, aimed at continuing studies on dielectric integration on 2D materials.

Collaborations

Das Research Group, Department of Engineering Science and Mechanics, Penn State University (USA): joint research on 2D semiconductors and device physics.

2D Crystal Consortium – Materials Innovation Platform, Penn State University (USA): use of samples provided by Prof. Joan M. Redwing.

Department of Inorganic Chemistry, University of Chemistry and Technology, Prague (Czech Republic): access to high-quality TMDs crystals provided by Prof. Zdeněk Sofer.

Other

Supervisor of the Bachelor of Science thesis at Faculty of Physics, Warsaw University of Technology: *Badanie wpływu kontaktów van der Waalsa na działanie urządzeń opartych na materiałach dwuwymiarowych* (2024).

Co-supervisor of the Bachelor of Science thesis at Faculty of Physics, Warsaw University of Technology: *Wytwarzanie heterostruktur van der Waalsa techniką polimerowych stempli* (2024).

List of figures

List of abbreviations

2D	Two-Dimensional
3D	Three-Dimensional
Al_2O_3	Aluminum Oxide
CB	Conduction Band
CVD	Chemical Vapor Deposition
DIGS	Defect-Induced Gap States
EOT	Equivalent Oxide Thickness
FLP	Fermi Level Pinning
hBN	Hexagonal Boron Nitride
HfO_2	Hafnium Dioxide
I_{SD}	Source-Drain Current
LCR	Inductance–Capacitance–Resistance (Meter)
MIGS	Metal-Induced Gap States
MoS_2	Molybdenum Disulfide
MOCVD	Metal-Organic Chemical Vapor Deposition
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PDMS	Polydimethylsiloxane
PEALD	Plasma-Enhanced Atomic Layer Deposition
PMMA	Poly(methyl methacrylate)
RIE	Reactive Ion Etching
SiO_2/Si	Silicon Dioxide on Silicon
SMU	Source Measure Unit
SS	Subthreshold Swing
TLM	Transfer Length Method
TMD	Transition Metal Dichalcogenide
V_{BG}	Back-Gate Voltage
VB	Valence Band
vdW	van der Waals
V_{DS}	Drain–Source Voltage
V_{GS}	Gate Voltage
V_{TG}	Top-Gate Voltage
WSe_2	Tungsten Diselenide

WS_2	Tungsten Disulfide
ZrO_2	Zirconium Dioxide